The Multi-FPGA Prototyping Platform

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The DINI Group

• We make big FPGA boards

• Most common application is prototyping
Issues FPGA Prototyping

- Large FPGA boards are hard to design and harder to build
  - Worse, in house boards are built in small quantity
- Partitioning
- Debug
Overview of Prototyping Product Line

• Goal: Provide customers a cost-effective vehicle to use the biggest and fastest FPGAs
  – Xilinx: Virtex-5, Virtex-6
  – Altera Stratix-4

• We try to keep lead-times under 2-3 weeks.
  – If not 2 weeks, issue is usually availability of FPGAs
    • Supply issues starting to ease
Xilinx Virtex-6

• Shipping with Virtex-6:

  – PCIe
    • DN-DualV6-PCIe-4 – 2 FPGAs (SX475T/LX365T et al.)
    • DNV6_F6_PCIe – 2 FPGAs (LX760/LX550T)
    • DNV6F6PCIe – 6 FPGAs (LX550T/SX475T et al.)

  – Standalone
    • D2076k10 – ‘Monster's Refrigerator Repairman’
      – 22 layers (don’t need 40)
      – 7 FPGAs (LX760/LX550)
Altera Stratix-4

• Now shipping production Altera S4 4SE820
  – PCIe
    • DN7406k10PCIe-8T
      – 6, 4SE820 FPGAs
  – Standalone
    • DN7020k10 – Uncle of Monster
      – 20 FPGAs (4SE820)
    • DN7002k10MEG – SOC Prototyping,
      – 2 FPGAs (4SE820)
Altera Stratix IV – 130M ASIC gates
Uncle of Monster
Uncle of Monster – DN7020k10
Features of DINI FPGA boards
FPGAs

- Largest package is the 1760 FFG
  - Typically ~1200 I/O’s

- Xilinx Virtex-6 LX760 is ~5.5 million ASIC gates
  - LX550T is ~4 million ASIC gates
• How gates calculated in Virtex-6:
  – (6-input LUT/FF pairs) * 16 -- About 16 gates for LUT/FF pair
  * 1.2 (for extra FF) -- From benchmarks extra FF is ~20%
  * .60 (60% utilized) -- Reasonable 60% utilization

Example (LX760): 474240 * 16 * 1.2 * .6
                   = 5.5 Mgates+ memory+ multipliers
Frequency: FPGA vs. ASIC

• FPGA speed is dependent on the design
  – In equal process geometry
    – V6/S4 is 40nm
  • FPGA will run at 1/10 frequency
    – With NO work at all.
  • FPGA will run a 1/5 frequency
    – With a little effort such as constraint files …
  • FPGA will run near ASIC speed
    – With a *lot* of effort …
Marvell MV78200

- Configuration processor is a Marvell MV78200
  - Dual ARMv5TE cores (clocked at 1 Ghz)
  - Floating point
  - 128M x 64 external memory
  - Many peripheral interfaces
    - USB/Ethernet/SATA II/PCIe
  - Boots to Linux
MV78200 -- Interfaces

[Diagram showing various interfaces and connections for MV78200]

- 10/100/1000 baseT
- RJ45
- RS232
- USB 2.0 (3x)
- SATA II (host) 2x
- FPGA G
- OSC
- MPP Bus
- PCIe (Gen1) 4 - lanes
- Third Party debug connector
- 128M x 64 DDR2
- 128Mb SPI Boot FLASH
- 256Mb NAND FLASH Boot
- PCI Express Cable (GEN 1)
EMU

- EMU – A full GUI interface
- Configure FPGAs, clocks, run tests etc.
Config FPGA and *NMB* Bus

- Massive data throughput between Marvell processor and FPGAs via *NMB* busses
  - Intended for user access to each FPGA from PCIe.
  - Point to point 10-signal LVDS bus
    - 1 Gb/s per signal
    - Includes DMA engines
    - Great for future debug
SODIMM’s

• Memory expansion is done with DDR3 SODIMM sockets
  – Additional, add-on cards not necessary
  – 204-pin
  – 64-bit data path
  – ~120 total signals
  – Up 2GB is cheap. 4GB is quite expensive
  – 533MHz (PC3-8500)

• Remember that each FPGA has block memory
Alternate SODIMM’s …

• DDR3 SODIMM connections consist of:
  – clocks
  – Power and GND
  – FPGA I/O’s (~120 or so)

• We can redefine this interface for different types of memories and functions
Compatible SODIMM: SSRAM

- 1M/2M x 64 Synchronous SRAM
- Mictors
- Interconnect
- Flash/SSRAM
- Mobile SDRAM and Flash
- QDR
- RLDRAM I/II
Compatible SODIMM: SSRAM

- USB 2.0 Phy
- DDR2
- DDR1/SDR SODIMM
Expansion and Customization

- Customization accomplished using expansion connectors on back
  - FCI MEG-ARRAY (non-proprietary)
    - Low insertion force
  - 400-pin grid of balls
  - 10 GB/s diff. performance
  - 96 LVDS pairs (192 single-ended)
  - +Power, ground, clocks
- Largely compatible across product lines
  - When (if) differences, they are related to frequency
Debug

• Debug is difficult and time consuming on FPGA-based prototypes
  – Normally done with embedded logic analyzers attached to JTAG chain
    • ChipScope (Xilinx)
    • SignalTap (Altera)

• Third party solutions coming soon …….
Conclusion

• Big, cool FPGA boards
  – Altera, Xilinx
• Short lead-time
• I’m back at 3:30pm to talk about HPC