

FPGA-based SOC Verification

The seminar will discuss the issues related to implementing system-on-a-chip (SOC) intellectual property (IP) using FPGA's. The following topics will be addressed:

FPGA selection

Which FPGA vendors' technology best suits FPGA implementations of SOC? Device families from Xilinx, Altera and others will be covered. Some rules for estimating the device size along with a brief discussion of what FPGA speeds to expect. Some formulas will be presented to estimate the amount of FPGA logic needed, which should help in selecting the correct target device.

What to look out for when doing an FPGA conversion

As always, some problems can occur when implementing IP designed for an ASIC into an FPGA. Generally all the memories must be adapted. Clock distribution can be a can of worms. Large designs must be partitioned across multiple FPGA's. Some general design suggestions will be presented that will ease the transition to FPGA's by making the RTL friendlier to FPGA's.

Which tools to use

The verilog vs. VHDL issue will be addressed along with suggestions for simulation, synthesis, place/route, and in-system debugging.

Existing Platforms

An overview of HW options for hosting the verification will be discussed. Several good off-the-shelf solutions are available in addition to user-designed custom boards.