

## Errata 1.0 Problems with configuration of FPGA's ABCDE

Some initial PWB's were shipped with a series termination resistor on CCLK that was too large for the load. This caused a transmission related hump in the rising edge of this clock and caused problems with the configuration mechanism on five of the Xilinx parts.

Workaround:

1. Replace resistor network RN9 with a 10 ohm value.
2. Solder a wire across pins 1 and 8. (See diagram)

