



Important Product Information



DEVICE ERRATA Virtex-II Pro Family

Dear Xilinx Customer,

Thank you for your interest in the enclosed Virtex-II Pro devices.

The Device Errata and Operational Guidelines apply to all Virtex-II Pro production devices (in all package types).

General Description

This errata affects only designs that use the CLK2X output as the feedback clock for a DCM. Designs that use the CLK2X output but do not use it as the feedback clock are not affected. If a design uses the CLK2X output as the feedback clock for a DCM, the LOCKED output can go low and the DCM can stop operating correctly. At present there are no plans to change the device. To eliminate the risk of this behavior, the solution below should be implemented.

Solution

1. If the design already uses CLK0 to drive a BUFGMUX, then use the output of this BUFGMUX to drive the CLKFB pin instead of the BUFGMUX that is connected to the CLK2X clock. There is no difference in performance. Also, change the CLK_FEEDBACK attribute from 2X to 1X.
2. If CLK0 is not used (not routed), but a BUFGMUX resource is available, then connect CLK0 to the available BUFGMUX and use its output to drive the CLKFB of the DCM, instead of to the BUFGMUX that is connected to the CLK2X clock. There is no difference in performance. Also, change the CLK_FEEDBACK attribute from 2X to 1X.
3. If CLK0 cannot be routed to an available BUFGMUX resource (as in solution 2), contact your local FAE or the Xilinx Hotline (http://www.xilinx.com/support/services/contact_info.htm) for alternative solutions.