

DN8000k10PCIE8 Errata

Last update: April 19, 2007

1) Symptom/Problem:

The compact flash card cannot be read directly after insertion.

Solution:

The compact flash card is not hot swappable. Turn the power off, insert the card, and then turn the power on.

2) Symptom/Problem:

Revision 1 boards only have this problem

The names of the signals connecting the FPGA and the Genesys GL9714 are incorrect: channels C and D on the connection to each GL9714 device have "RX" net names connected to "TX" signals on the GL9714 and "TX" nets connected to the "RX" pins on the GL9714.

Impact:

The names of the nets do not effect the correct operation of the interface.

Solution:

The schematic was corrected as of July 7, 2006. "TX" signals are driven by the FPGA. "RX" signals are driven by the GL9714. Dini Group recommends naming the signals within the FPGA design to reflect these changes.

3) Symptom/Problem:

Revision 1 boards only have this problem

PCIE2_PCLK is not connected to a global clock input pin. The signal PCIE2_PCLK, intended for synchronizing the interface between FPGA A and the second Genesys Logic 9417 (U6), is not connected to a Virtex-4 "GC" global clock input pin. As a result, it cannot be used reliably as a clock signal in the FPGA design.

Impact:

PCI express 8-lane operation cannot be used.

Solution:

Previous suggestions for correcting this problem included using the signal PCIE_PCLK signal for synchronously communicating with both GL9714 devices. This method has been shown to be unreliable, because the phase relationship between PCIE_PCLK and PCIE2_PCLK can change when the GL9714 goes into power-down mode.

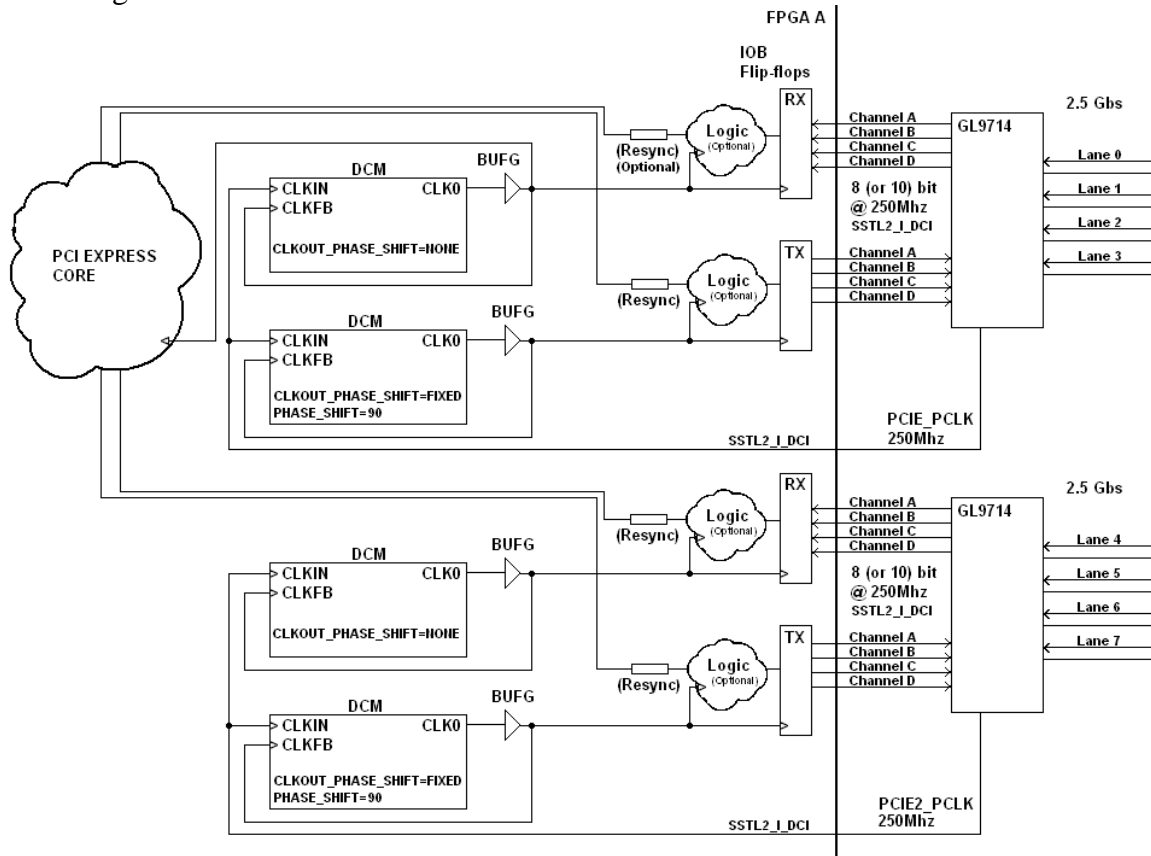
Dini Group may elect to upgrade you board to a revision 2. Please contact Dini Group.

The current work-around requires a rework wire to be added to your board to connect the PCIE2_PCLK signal to a "GC" pin on the Virtex-4 device. The Dini Group will

implement this rework on your board at your request.
 After the rework, the signal PCIE2_PCLK will connect to
 FPGA pin AP22 (and not AW15).

**Since AP22 connects to the Header A signal HAP75, this signal should not be used
 on the header.**

When using the work-around or a rebuilt board, the validated clocking scheme is shown
 in the diagram below. The new clocking scheme is also described in the latest version of
 the user guide.



4) The recommended clocking scheme for the GL9714 interfaces has changed. See the
 above errata for details.

5) The GL9714 PCI Express PHY devices require a heat sink. Without a heat sink, the
 devices' temperatures can exceed their guaranteed operational conditions. The Dini
 Group will repair and return your board if desired.

6) The DN8000K10PCIE8 is not compatible with the "16 bit" modes of the GL9714.
 This means the parallel interface must operate at 250Mhz.

7) The PHY layer is not responsible for lane-alignment ("channel-bonding"). The
 GL9714 does not do any lane-alignment. This must be accomplished on the MAC layer
 in the FPGA. Your PCI Express core probably supports this.

8) DCD and DCC signals on the interface to the GL9714 are mis-named. The "RXDKD" signal actually connects to the "RXDKC" pin on the GL9714 and the "RXDKC" signal actually connects to the "RXDKD" pin on the GL9714. On Sept 7, 2006, the schematic was changed so the net names reflect the signal function. The new signal names are
PCIe_RXDKC_NEW,
PCIe_RXDKD_NEW,
PCIe2_RXDKC_NEW,
PCIe2_RXDKD_NEW

9) Symptom/Problem:

Communication over MainBus is failing with one or more bits of the AD bus either inconsistent or stuck.

Solution:

Set the drive strength for all MainBus lines to 24mA. With the MainBus clock running at 48Mhz and with FPGA drivers set to lower than 12mA drive strength, failures on MainBus have been observed.