

DN9000K10PCI Errata

Last update: January 21, 2008

1) Differential Polarity On Daughtercards

Symptom/Problem

The signals DCE1N29, DCF0n02, DCF0n03 connect to “P” pins on the FPGA, and the signals DCE1P29, DCF0P02, DCF0P03 connect to “N” pins on the FPGA.

Impact

Only customers who are using one of these three pairs as a differential signal are affected. Single-ended use of these signals is not impacted.

Solution/Work-Around

When using daughtercards requiring differential signaling on these pins, then the FPGA RTL must invert the transmitted or received logic. The differential input buffer should connect so that the .I connects to a “P” pin on the FPGA, and the .IB port connects to an “N” pin on the FPGA.

2) 1.8V Power Sucks

Symptom/Problem:

DIMM B and DIMMC1 are under voltage.

Impact:

DN9000K10PCI boards which are “revision 2” which were shipped before January 10, 2008 are affected.

The under voltage occurs if and only if *both* DIMM B and DIMM C1 are being used at the same time. If you are not using *both* DIMM B and DIMM C1 in your design, you can ignore this problem.

Although the under voltage will likely not result in failure or performance limitations within the DDR2 memory itself (because the interface is being run at nearly half the rated speed), if you are using both DIMM B and DIMM C1 we recommend addressing the issue to avoid the possibility.

Solution:

Dini Group can trim up the voltage of the 1.8V rail such that under all conditions, the voltage remains within the DDR2 recommended operating conditions. In order to make this correction, the resistor R462 should be removed and replaced with an 11.0K (1%) resistor.

DN9000K10PCI boards with are “revision 2” and were shipped after January 10, 2008 already have the necessary modification.