

# Phy Daughter Card

## Frequently Asked Questions (FAQ)

(Updated 4/30/03)

**Q: Does the Xilinx chip on the daughtercard have a fixed functionality, or is it up to us to implement any MAC-like features in it?**

The Xilinx chip is programmable through the freely available tools from Xilinx (they are excellent). They support schematic capture, verilog and VHDL. The Xilinx chip (CPLD) comes programmed with an application that formats the raw frames in 16 bit words to be sent to the XC4000 on the main board. You can put anything you like in the CPLD but I would recommend putting the MAC on the XC4000 rather than the CPLD.

**Q: The block diagram seems to indicate that there is a well-defined interface, similar to the GMII between the daughtercard and the main board. Should we plan on implementing/purchasing a Gigabit Ethernet MAC IP core to control the Intel PHY, or is that part already implemented on the XC95144 ?**

The interface between the main board and the PHY card is like the GMII with the following differences:

- 1) the data width is always 16 bits rather than 8, 4 and 1 (1000,100,10); the clock is adjusted accordingly to 62.5,6.2, and 0.62 respectively.
- 2) there is no MMDIO (the serial management interface)

There is no MAC functionality either in the XC95144 or the XC4000; we are currently working with raw Ethernet frames. The XC95144 generates a FRAME pulse (in addition to the GMII signals) that marks the beginning of an Ethernet frame.