DNBC
Dini Bank Connection Interface Specification

Revision 1.5
Written 2015-01-01, A. Sikes
Dini Group, Inc.
Last Updated 2017-06-22, N. Harder
Copyright (c) 2015, 2016 Dini Group, Inc.

Contact:
Dini Group, Inc.
7469 Draper Ave
La Jolla, CA 92037
United States
Phone: (858) 454-3419

Support: support@dinigroup.com
Sales: sales@dinigroup.com
Web: http://www.dinigroup.com
# Table of Contents

1. Overview .................................................................................................................. 6  
   1.1 Other Files ........................................................................................................ 6  
   1.2 Terminology & Style ......................................................................................... 6  
   1.3 Revision History .............................................................................................. 7  
   1.4 Contact .............................................................................................................. 7  
2. Electrical Requirements ......................................................................................... 9  
   2.1 Signal and Pinout Description ........................................................................... 9  
      2.1.1 Signal Class Definitions ........................................................................... 13  
      2.1.2 Signal Connection Requirements ............................................................. 15  
   2.2 Signaling Standards, Level Tolerance, and Routing Requirements for Class 3 Signals 16  
      2.2.1 Signaling Standards and Termination for Class 3 Signals .......................... 16  
      2.2.2 Signal Routing Requirements ................................................................. 18  
   2.3 Interface Clocking Requirements .................................................................... 18  
      2.3.1 Mother Board Clock Inputs ...................................................................... 19  
      2.3.2 Clock Pin Selection ..................................................................................... 19  
   2.4 Cable Interface Requirements ......................................................................... 19  
   2.5 Daughter Board Interface Requirements ....................................................... 19  
   2.6 Memory Interface Requirements ................................................................... 20  
      2.6.1 Byte Group Pin Map ................................................................................. 20  
      2.6.2 Memory Interface Pin Assignments ......................................................... 21  
      2.6.3 Data vs Control Pin Placement ................................................................ 22  
      2.6.4 Clock Placement ....................................................................................... 22  
      2.6.5 Routing Requirements .............................................................................. 22  
   2.7 Power Provision & Control Signals ................................................................ 22  
      2.7.1 Hot Plugin .................................................................................................. 22  
      2.7.2 +12VDC Power Rail .................................................................................. 22  
      2.7.3 +12VDC Power Return Rail ..................................................................... 22  
      2.7.4 V_{CC0} Rail .............................................................................................. 23  
      2.7.5 Ground Pins .............................................................................................. 24  
      2.7.6 Control Signals ......................................................................................... 24  
   2.8 DNBC Daughter Board Configuration Interface .............................................. 25  
      2.8.1 Configuration Signal Interface ................................................................. 25  
      2.8.2 Signal Descriptions ................................................................................... 26  
      2.8.3 Signal Levels and Standards .................................................................... 27  
      2.8.4 Power Sequencing ..................................................................................... 27  
3. Mechanical Requirements ..................................................................................... 29
Table of Figures

Figure 1 - DNBC Interface Header Pinout ................................................. 10
Figure 2 - DNBC Mother Board Header Schematic Symbol ........................................... 13
Figure 3 - Byte Group Pin Map for DNBC Interface ........................................... 21
Figure 4 – Mother Board VCCO_SET Circuitry ........................................... 25
Figure 5 - DNBC Configuration Header ........................................... 26
Figure 6 - DNBC Configuration Sub-Interface ........................................... 26
Figure 7 - SEAM/SEAF Marketing Illustration ........................................... 29
Figure 8 - Illustration of LEFT Mother board DNBC Arrangement ........................................... 30
Figure 9 - Illustration of RIGHT Mother board DNBC Arrangement ........................................... 31
Figure 10 - Illustration of DNBC3 Daughter Card Outline ........................................... 34
Figure 11 - Illustration of Alternate DNBC Daughter Card Outlines ........................................... 35
Figure 12 - Example Layouts for DNBC3 Daughter Boards ........................................... 36
Figure 13 - Illustration of Stack for all DNBC Applications ........................................... 37
Figure 14 - Board Mezzanine Stack Assembly Illustration ........................................... 38
Figure 15 - Illustration of Double-Wide Board Outline ........................................... 39
Figure 16 - Illustration of Daughter Board Cabling ........................................... 40

Appendix A. Design Check Lists................................................................. 41
   A.1. Mother Board Check List................................................................. 41
   A.2. Daughter Board Check List................................................................. 42
Table of Tables

Table 1 - Single-Ended Signaling Standard Voltage Level Definition ................................................................. 17
Table 2 - LVDS Voltage Level Definition ........................................................................................................ 17
Table 3 - Cable Signal Mapping ......................................................................................................................... 32
1. Overview
This document describes the DNBC (Dini Bank Connection) bank expansion interface. Mechanically, each DNBC interface consists of six identical 120-pin connectors on a mother board that have the following characteristics:

- All six connectors connect to a single FPGA on the mother board. With Xilinx FPGAs, each connector interfaces to a single SelectIO bank, bringing out 24 differential pairs plus four single-ended I/O signals, VCCO for the FPGA bank, +12VDC power and power management signals.
- Individual connectors may be cabled to DNBC connectors on the same mother board or to other mother boards, using a 120-pin custom micro-coax cable for high-performance system interconnect. Each DNBC interface may be used to connect up to 312 signals to as many as 6 remote mother boards.
- A DNBC3 daughter board mounts as a mezzanine board on the first three DNBC connectors while leaving the other three connectors free for interconnect. The daughter board provides approximately 12 square inches for expansion circuitry and connects up to 156 FPGA signals.
- Alternate daughter board profiles may connect to one (DNBC1), two (DNBC2) or all six (DNBC6) interface connectors.

Electrically, the interface is comprised of a number of user-definable digital signals, including several clocks inputs, and power distribution and management signals.

This specification also defines a 14-pin header/ribbon cable interface to allow an FPGA on a daughter board to be configured from the mother board.

The goal of the DNBC interface is to specify a flexible and modular expansion interface that can be used to augment the functionality of off-the-shelf Dini Group ASIC Emulation systems. The principal use model is to customize features and interfaces available on a Dini Group ASIC emulation mother board, which itself hosts one or more FPGAs, with additional memories, off-board interfaces, ADC, and DACs. Thus, the ASIC emulation system can be tailored to support an end-user’s desired feature mix.

The DNBC interface allows for one standard daughter board physical outline and three alternate outlines, but custom alternatives may include dual DNBC daughter boards. Section 3 describes the physical outline options.

The DNBC interface is primarily intended to be used on Dini Group Xilinx UltraScale ASIC emulation products, but can also be used on Altera baseboards or retrofitted onto baseboards with older Xilinx technologies. It is not backwards compatible with the Dini Group DINAR1 or MEG Array expansion interfaces such as that found on the Dini Group Virtex-7 and older ASIC emulators.

1.1 Other Files
This specification makes reference to several files and drawings. They are enumerated here:

1. DNBC Mechanical.vsd – an annotated set of drawings describing the DNBC daughter board form factor.

1.2 Terminology & Style
A variety of terminology is used throughout this document. Some of it has very specific meaning.

The phrases are to/shall/required/must state hard requirements for all cards implementing the DNBC interface. The words highly recommended denote characteristics that are not hard requirements, but should be implemented where possible and are likely to become requirements in future major revisions of the DNBC specification. The word recommended denotes characteristics that are not hard requirements nor likely to become such, but should be implemented where reasonable.
The terms “mother board,” “main board,” “baseboard” and “host” are used interchangeably, and refer to the FPGA-based Dini Group ASIC emulation board. The term “daughter board” refers to the smaller mezzanine-mounted expansion board.

The phrases “DNBC Interface” and “DNBC Slot” are used interchangeably to refer to each 6-connector DNBC connector pattern on a mother board. The phrases “DNBC1”, “DNBC2” and “DNBC3” refer, respectively, to DNBC daughter boards with one, two and three interface connectors.

1.3 Revision History

0.1 – 2015-01-30, A. Sikes
1. Initial Revision

0.2 – 2015-02-02, A. Sikes
1. Delete PWR_GD, both on the connector pinouts and in the text. Use power-on timeout instead.

0.3 – 2015-03-05, A. Sikes
1. Added Section 3.7.6, Daughter Board Power Monitoring
2. In Figure 1, swapped the “RXnp” and “RXnn” pin assignments to match the cable.
3. Updated mechanical figures to correct connector order and tweak board dimensions.
4. Made numerous editorial changes and clarifications.

0.4 – 2015-04-07, A. Sikes
1. Various changes throughout to clarify text and figures.
2. Added discussion of SE0/VRP pin in Section 2.1.2.
3. Added Section 2.1.2.1 FPGA Bank Selection.
4. Added Section 2.7.1 Hot Plugin.
5. Added Configuration header description in Section 3.5 and expanded cable description.
6. Added diagram in Section 3.7.4 Daughter Board Cabling.

0.5 – 2015-04-10, A. Sikes
1. Changed document type from pdf to vsd in Section 1.1.
2. Clarified depopulation of mother boards in Section 2.1.2.3.
3. Removed cable details in Section 2.4 and cross-referenced Section 3.3.
4. Clarified that hot plugin only can apply to cables, not daughter boards in Section 2.7.1.
5. Added cable PIDs in Section 3.5.

0.6 – 2015-05-12, A. Sikes
1. Added warnings in Section 2.1.2 about the B1S13P/B1S13N and VREF pins. Expanded the VRP warning.
2. Clarified Section 3.7.2 and 3.7.3 as pertaining only to adjacent positions “on the same FPGA.”
3. Added the reason to have a +12V LED on daughter boards to Section 3.7.6.
4. Added Appendix A, Design Check Lists.

0.7 – 2015-07-28, A. Sikes
1. Changed the configuration header in Section 2.8.1 from 0.1” to 2mm and added the recommended part number.
2. Added Section 2.8.2.6 defining the VREF signal at the configuration interface.

1.0 – 2015-08-12, A. Sikes
1. In Section 2.8.2, changed all the mother board pull-down resistors from 4.7K to 10.0K and the daughter board pullup resistors from 470 ohm to 1.00K.
1.1 – 2015-10-20, A. Sikes
   1. Modified Figure 13 and Section 3.6.2.2 to use M3 hardware for the stack rather than 4-40.

1.2 – 2016-02-10, A. Sikes
   1. Modified Figure 2 to correct the nomenclature at pin 2-59 from B1_TX9P_S10P_DQS1N to B1_TX9N_S10N_DQS1N.

1.3 – 2016-03-17 A. Sikes
   1. Modified Sections 3.6.2.2 and 3.6.2.3 to recommend Phillips-head screws rather than Allen-head screws and to delete the washers.

1.4 – 2016-08-26 A. Sikes
   1. Modified Sections 3.4 and 3.6.2.1 to explain the height restrictions on the front of the board.

1.5 – 2017-06-22 N. Harder
   1. Modified schematic symbols in Section 2.1 to just say “+1.0V - +1.8V” on all 6 connectors. Before it erroneously said +1.8V only for connectors 4-6, and connectors 1-3 said “2A max from daughterboard” which was rather confusing even if technically correct.
   2. In section 3.2 inserted a note that the DNVUF1A, DNVUF2A, and DNVUF4A do not correctly number the “RIGHT” DNBC positions.

1.4 Contact
For questions or comments regarding the interface specification, contact support@dinigroup.com.
2. Electrical Requirements
This section will define electrical requirements for the DNBC interface. Enumerated will be requirements for signals, including signaling standards and routing requirements, as well as description of the logical interface requirements such as synchronous I/O timing information. Also in this section non-signal electrical requirements, i.e. power distribution, will be described.

2.1 Signal and Pinout Description
All six connectors for each DNBC interface have identical pin assignments. This section will describe the signals and pinout for a single connector.

A pinout of the DNBC interface connector is given below, both when used as a cable interface and when used for a daughter board. Pin numbers follow the SEAM/SEAF pin numbering convention. All pin names ending with ‘p’ represent the true component of a differential signal. All pin names ending with ‘n’ represent the complementary component of a differential signal.
### Cable

<table>
<thead>
<tr>
<th></th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>GND</td>
<td>TX0n</td>
<td>TX0p</td>
<td>TX0v</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX1n</td>
</tr>
<tr>
<td>16</td>
<td>TX1p</td>
<td>GND</td>
<td>TX1n</td>
<td>GND</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX2n</td>
</tr>
<tr>
<td>24</td>
<td>TX2p</td>
<td>GND</td>
<td>TX2n</td>
<td>GND</td>
</tr>
<tr>
<td>28</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX3n</td>
</tr>
<tr>
<td>32</td>
<td>TX3p</td>
<td>GND</td>
<td>TX3n</td>
<td>GND</td>
</tr>
<tr>
<td>36</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX4n</td>
</tr>
<tr>
<td>40</td>
<td>TX4p</td>
<td>GND</td>
<td>TX4n</td>
<td>GND</td>
</tr>
<tr>
<td>44</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX5n</td>
</tr>
<tr>
<td>48</td>
<td>TX5p</td>
<td>GND</td>
<td>TX5n</td>
<td>GND</td>
</tr>
<tr>
<td>52</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX6n</td>
</tr>
<tr>
<td>56</td>
<td>TX6p</td>
<td>GND</td>
<td>TX6n</td>
<td>GND</td>
</tr>
<tr>
<td>60</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX7n</td>
</tr>
<tr>
<td>64</td>
<td>TX7p</td>
<td>GND</td>
<td>TX7n</td>
<td>GND</td>
</tr>
<tr>
<td>68</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX8n</td>
</tr>
<tr>
<td>72</td>
<td>TX8p</td>
<td>GND</td>
<td>TX8n</td>
<td>GND</td>
</tr>
<tr>
<td>76</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX9n</td>
</tr>
<tr>
<td>80</td>
<td>TX9p</td>
<td>GND</td>
<td>TX9n</td>
<td>GND</td>
</tr>
<tr>
<td>84</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX10n</td>
</tr>
<tr>
<td>88</td>
<td>TX10p</td>
<td>GND</td>
<td>TX10n</td>
<td>GND</td>
</tr>
<tr>
<td>92</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX11n</td>
</tr>
<tr>
<td>96</td>
<td>TX11p</td>
<td>GND</td>
<td>TX11n</td>
<td>GND</td>
</tr>
<tr>
<td>100</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>SE0/VRP</td>
</tr>
<tr>
<td>104</td>
<td>SE0/VRP</td>
<td>GND</td>
<td>GND</td>
<td>SE1/VREF</td>
</tr>
<tr>
<td>108</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>SE2/VREF</td>
</tr>
<tr>
<td>112</td>
<td>SE3/VREF</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>116</td>
<td>VCCO</td>
<td>GND</td>
<td>GND</td>
<td>VCCO</td>
</tr>
<tr>
<td>120</td>
<td>PWR_ON</td>
<td>GND</td>
<td>GND</td>
<td>VCCO</td>
</tr>
</tbody>
</table>

### Daughter Board

<table>
<thead>
<tr>
<th></th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX0p</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX1n</td>
</tr>
<tr>
<td>16</td>
<td>TX1p</td>
<td>GND</td>
<td>TX1n</td>
<td>GND</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX2n</td>
</tr>
<tr>
<td>24</td>
<td>TX2p</td>
<td>GND</td>
<td>TX2n</td>
<td>GND</td>
</tr>
<tr>
<td>28</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX3n</td>
</tr>
<tr>
<td>32</td>
<td>TX3p</td>
<td>GND</td>
<td>TX3n</td>
<td>GND</td>
</tr>
<tr>
<td>36</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX4n</td>
</tr>
<tr>
<td>40</td>
<td>TX4p</td>
<td>GND</td>
<td>TX4n</td>
<td>GND</td>
</tr>
<tr>
<td>44</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX5n</td>
</tr>
<tr>
<td>48</td>
<td>TX5p</td>
<td>GND</td>
<td>TX5n</td>
<td>GND</td>
</tr>
<tr>
<td>52</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX6n</td>
</tr>
<tr>
<td>56</td>
<td>TX6p</td>
<td>GND</td>
<td>TX6n</td>
<td>GND</td>
</tr>
<tr>
<td>60</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX7n</td>
</tr>
<tr>
<td>64</td>
<td>TX7p</td>
<td>GND</td>
<td>TX7n</td>
<td>GND</td>
</tr>
<tr>
<td>68</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX8n</td>
</tr>
<tr>
<td>72</td>
<td>TX8p</td>
<td>GND</td>
<td>TX8n</td>
<td>GND</td>
</tr>
<tr>
<td>76</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX9n</td>
</tr>
<tr>
<td>80</td>
<td>TX9p</td>
<td>GND</td>
<td>TX9n</td>
<td>GND</td>
</tr>
<tr>
<td>84</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX10n</td>
</tr>
<tr>
<td>88</td>
<td>TX10p</td>
<td>GND</td>
<td>TX10n</td>
<td>GND</td>
</tr>
<tr>
<td>92</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>TX11n</td>
</tr>
<tr>
<td>96</td>
<td>TX11p</td>
<td>GND</td>
<td>TX11n</td>
<td>GND</td>
</tr>
<tr>
<td>100</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>SE0/VRP</td>
</tr>
<tr>
<td>104</td>
<td>SE1/VREF</td>
<td>GND</td>
<td>GND</td>
<td>SE2/VREF</td>
</tr>
<tr>
<td>108</td>
<td>SE3/VREF</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>112</td>
<td>VCCO</td>
<td>GND</td>
<td>GND</td>
<td>VCCO</td>
</tr>
<tr>
<td>116</td>
<td>PWR_ON</td>
<td>GND</td>
<td>GND</td>
<td>VCCO</td>
</tr>
<tr>
<td>120</td>
<td>VCCO_SET</td>
<td>GND</td>
<td>GND</td>
<td>VCCO</td>
</tr>
</tbody>
</table>

---

**Figure 1 - DNBC Interface Header Pinout**
The figure below shows the schematic symbol for the DNBC mother board header (nominally six Samtec SEAF-30-05.0-L-04-2-LP-K connectors, see section 3.1). The daughter board header symbol is identical to the first three sections of the mother board symbol. Some annotation within the symbol is provided; this annotation will be clarified later in this document.
### DNBC Connector 3

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>B2_TXOP_001P_DM0</td>
<td>B2_RXOP_013P_DM2_GC</td>
</tr>
<tr>
<td>2</td>
<td>B2_TXOPN_001N_UAD</td>
<td>B2_RXOPN_103N_UAD2_GC</td>
</tr>
<tr>
<td>3-4</td>
<td>B2_TXOP_001P_DQ0</td>
<td>B2_RXOP_101P_DQ2</td>
</tr>
<tr>
<td>5-6</td>
<td>B2_TXOPN_001N_DQ0</td>
<td>B2_RXOPN_101N_DQ2</td>
</tr>
</tbody>
</table>

### DNBC Connector 4

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>B3_TXOP_001P</td>
<td>B3_RXOP_013P_GC</td>
</tr>
<tr>
<td>2</td>
<td>B3_TXOPN_001N</td>
<td>B3_RXOPN_103N_GC</td>
</tr>
</tbody>
</table>

---

**References:**

- SEAF-30-05-01-04-2-2U-2P-K-TR
- SEAF-30-05-01-04-2-2U-2P-K-TR

---

**Footer:**

Rev 1.5, 2017-06-22
Page 12 of 43
2.1.1 Signal Class Definitions

This section will group the signals into signal Classes, describe functionality and characteristics of the Classes, and define terminology associated with them. Signals may belong to several Classes at once.
Note that sections 2.1 through 2.3 make minimal mention of Class 1 and 2, “power” and “control” pins. These are specified in section 2.7. The Class 5 “configuration” pins are described in section 2.8.

2.1.1.1 Class 1 – Power
The Power pins include \( V_{CCO} \), \(+12\text{VDC}\) and \(+12\text{V}_{\text{RTN}}\).

2.1.1.2 Class 2 – Control
The Control pins are responsible for power sequencing and card detection. The control pins are \( \text{PWR\_ON} \) and \( \text{VCCO\_SET} \).

2.1.1.3 Class 3 – GPIO Signals
These are general purpose I/O pins that can be used to implement a variety of interfaces. Signal pins can be used as both single-ended (LVCMOS, SSTL, or HSTL) pins or as differential (LVDS) pin pairs. When used with FPGAs with unidirectional signals, the cable interface pinout shows the signals preferentially connected to transmit outputs (TXxxp/n) or to receiver inputs (RXxxp/n).

2.1.1.3.1 Class 3a – Byte Groups
Byte groups are groups of 12 pins each that form a single “byte lane”. Their most common use is for high-speed memory interfaces, such as DDR DRAM or QDR SRAM. Each byte lane consists of a differential strobe pair (DQS/DQSn), a data mask pin (DM), an unassigned pin (UA), eight data signals and a single-ended signal.

For a pin map that denotes the byte groups, as well as further discussion on employing a memory interface over the DNBC, see section 2.4.

All Class 3a pins are also Class 3 pins.

2.1.1.3.2 Class 3b – Clocks
Clocks can be used to clock an interface or an entire system containing the DNBC interface. All defined clocks propagate in the downward direction, that is, from daughter board to mother board. Any Class 3 signal pair may be used as an upward clock (to the daughter board).

When used on a Xilinx UltraScale motherboard, or mother boards based on similar FPGAs, all clock inputs at the DNBC interface connect to “global” clock inputs on the FPGA. For older technologies, such as Virtex 7, there are two types of clocks at the DNBC interface, system and local clocks. System clocks can be used to clock the entire interface\(^1\), local clocks can only be used to clock signals within the same bank.\(^2\)

All signals in Class 3b are also Class 3 pins.

2.1.1.3.3 Class 3c – Single-Ended Signals
These are general purpose I/O pins that can be used to implement a variety of interfaces. These pins can only be used as single-ended (LVCMOS, SSTL, or HSTL) pins. Three of the four Class 3c pins on each connector are also used for secondary purposes: one for the VRP reference resistor for I/O impedance calibration and two as optional external VREF pins.

All Class 3c pins are also Class 3 pins.

2.1.1.4 Class 4 - Ground
All ground pins are Class 4 pins. These are digital ground.

---

\(^1\) Typical implementation of system clocks is to use the FPGA MRCC pins for Xilinx 7-series parts.

\(^2\) Typical implementation of local clocks is to use FPGA SRCC pins for Xilinx 7-series parts
2.1.1.5 Class 5 – Configuration
Configuration signals are used to implement a serial configuration interface that allows the mother board to configure an FPGA hosted on a daughter board. These signals are defined as LVCMOS18 signals. They are not included on the six DNBC headers, but on a separate 14-pin header. They are not referenced to any of the VCCO pins on the daughter board nor to any other signals on the daughter board (except GND). These signals and the rules governing their function are described in Section 2.8.

2.1.2 Signal Connection Requirements
The mother board shall have all of the interface signals connected appropriately. Byte groups at the interface shall be connected to corresponding byte groups on the mother board host FPGA. Clocks shall be connected to FPGA clock inputs on the mother board FPGA. SE1/VREF and SE3/VREF shall optionally be connected to the one or two FPGA VREF input pins for the bank, in addition to normal I/O pins. The SE0/VRP pin at the DNTC interface is not normally connected to FPGA pins. Instead, the FPGA VRP pin is terminated on the mother board (see Section 2.1.2.2 below). This pin on each of the DNBC connectors shall not normally be used on a daughterboard, since a mother board modification will be required to connect it. Where a daughter board requires use of this pin, it shall clearly state the need to modify the mother board.

By default, the SE0/VRP pin at each DNBC connector is not connected to the mother board FPGA. A mother board modification is required to make them available for use as an I/O signal. If they are used for I/O signals, a warning should be present in the user manual for the daughter board.

The B1S13P/B1S13N SCK pair will have an external 100Ω resistor between them on the mother board that can only be removed by modifying the board. Do not use these pins for single-ended I/O (or in a pinch use only 1 of them). If they are used, a warning should be present in the user manual for the daughter board.

By default, the SE1/VREF and SE3/VREF pins at each DNBC connector can be used for single-ended I/O signals. However, mother board may optionally be modified to use these pins as VREF pins into the FPGA. If they are used for I/O signals, a warning should be present in the user manual for the daughter board.

A daughter board is not required to connect all Class 3 signals; unconnected signals shall be left floating. All Class 1, 2 and 4 signals must be implemented in accordance with section 2.7.

The DNBC Daughter Board Configuration interface is on a separate header and is not required as part of every DNBC interface. Typically, a single DNBC Configuration header is included on a mother board, or one for each User FPGA on the mother board. It is only used to configure FPGAs on DNBC daughter boards. See section 2.8.

2.1.2.1 FPGA Bank Selection
The FPGA banks connected to the first three DNBC connectors must be selected such that high-speed memory interfaces will function properly on daughter boards. Specifically, for Xilinx UltraScale FPGAs, this means that they must be consecutive banks in the same SLR, assigned in order (or reverse order). The FPGA banks connected to the last three DNBC connectors may be selected anywhere on the FPGA. Note that this means that having a memory interface on a DNBC6 daughterboard is not recommended, since the two groups of connectors will be swapped in certain mother board positions.
2.1.2.2 Impedance Control and VRP/VRN Pins
The VRP/VRN pins on a Xilinx FPGA (RZQ pins on Altera FPGAs) are used for impedance control and calibration for mother board I/O. By default, these pins are not brought out to the DNBC interface but are terminated on the mother board. Optionally, each of these signals shall be routed to the DNBC interface using zero ohm resistors. Specifically:

Xilinx UltraScale - The VRP pin in each interface bank is connected through a 499 ohm resistor to ground. An optional zero ohm resistor connects it to the SE0/VRP pin on the DNBC connector, for use as a Class 3c single-ended signal.

Xilinx V7/V6 - The VRP and VRN pins in each interface bank are shared as I/O pins connected to the DNBC interface. Optional calibration resistors on the mother board should connect the VRN pin to the Vcco of the relevant bank and the VRP pin to ground. If this feature is used, the resistors should be installed with 2R values, where R is the desired termination impedance. If the feature is not used, the I/O pins may be used as general purpose Class 3 pins on the daughter board.

Altera - The RZQ pin for each interface bank must be connected through a 100 or 240 ohm resistor to ground on the mother board. An optional zero ohm resistor connects it to the SE0/VRP pin on the DNBC connector, for use as a Class 3c single-ended signal.

2.1.2.3 Depopulation Order

The mother board is required to connect all signals on the DNBC interface. The rules in this section apply only to daughter board connections. If a non-compliant mother board is not able to connect all signals at a DNTC interface, it shall follow the following order in leaving signals unconnected and shall clearly indicate in its documentation that it has depopulated DNBC pins.

If a daughter board designer chooses to only partially connect a DNBC connector, it is highly recommended that a particular depopulation order be followed. The signals should be depopulated in the following order:

1. Byte group 0 should be depopulated in banks 2, 1, 0, in that order.
2. Byte group 3 should be depopulated in banks 2, 1, 0, in that order.
3. Remaining signals should be depopulated in banks 2, 1, 0, in that order.

In general, entire byte groups should be depopulated one at a time, before depopulating the next byte group.

2.2 Signaling Standards, Level Tolerance, and Routing Requirements for Class 3 Signals
This section defines the signaling standards to be employed, signaling levels to be tolerated, and physical routing requirements for Class 3 (non-configuration/power) signals. In general, the approach for the mother board side of the interface is to be as flexible as possible, making provisions for both single-ended and differential signaling, minimizing skew between pairs and maximizing interface access to clock resources. The daughter board design is typically more constrained as the daughter board is geared towards implementing a specific interface.

2.2.1 Signaling Standards and Termination for Class 3 Signals
This section defines the signaling standards applicable to Class 3 signals.

All Class 3 signals shall tolerate a single-ended voltage of between -0.3V to Vcco + 0.3V.

The mother board shall be capable of bi-directional signaling on all Class 3 signals. It shall both accept and transmit either LVCMOS, SSTL, HSTL, or LVDS levels. Vcco may be between +1.00VDC – 5% and +1.80VDC + 5%. The daughter board design shall determine the signaling standard to use and the
daughter board will therefore provide an appropriate $V_{CCO}$ voltage within the defined range or can use the $VCCO_{SET}$ pin to set the output voltage of the $V_{CCO}$ bias regulator on the motherboard (see Section 2.7.6.4).

Single-Ended signaling levels, relative to the motherboard I/O pins, are defined in the following table.

Table 1 - Single-Ended Signaling Standard Voltage Level Definition

<table>
<thead>
<tr>
<th>Signaling Std</th>
<th>$V_{IL_{MIN}}$</th>
<th>$V_{IL_{MAX}}$</th>
<th>$V_{IH_{MIN}}$</th>
<th>$V_{IH_{MAX}}$</th>
<th>$V_{OL_{MAX}}$</th>
<th>$V_{OH_{MIN}}$</th>
<th>$I_{OL}$ (mA)</th>
<th>$I_{OH}$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSTL I</td>
<td>-0.300</td>
<td>$V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$VCCO + 0.300$</td>
<td>0.4</td>
<td>$VCCO - 0.400$</td>
<td>5.8</td>
<td>-5.8</td>
</tr>
<tr>
<td>HSTL I_12</td>
<td>-0.300</td>
<td>$V_{REF} - 0.080$</td>
<td>$V_{REF} + 0.080$</td>
<td>$VCCO + 0.300$</td>
<td>25% $VCCO$</td>
<td>75% $VCCO$</td>
<td>4.1</td>
<td>-4.1</td>
</tr>
<tr>
<td>HSTL I_18</td>
<td>-0.300</td>
<td>$V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$VCCO + 0.300$</td>
<td>0.4</td>
<td>$VCCO - 0.400$</td>
<td>6.2</td>
<td>-6.2</td>
</tr>
<tr>
<td>HSUL 12</td>
<td>-0.300</td>
<td>$V_{REF} - 0.130$</td>
<td>$V_{REF} + 0.130$</td>
<td>$VCCO + 0.300$</td>
<td>20% $VCCO$</td>
<td>80% $VCCO$</td>
<td>0.1</td>
<td>-0.1</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>-0.300</td>
<td>35% $VCCO$</td>
<td>65% $VCCO$</td>
<td>$VCCO + 0.300$</td>
<td>0.4</td>
<td>$VCCO - 0.400$</td>
<td>2/4/6/8 mA</td>
<td></td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>-0.300</td>
<td>35% $VCCO$</td>
<td>65% $VCCO$</td>
<td>$VCCO + 0.300$</td>
<td>0.45</td>
<td>$VCCO - 0.450$</td>
<td>2/4/6/8/12 mA</td>
<td></td>
</tr>
<tr>
<td>LVDCI 15</td>
<td>-0.300</td>
<td>35% $VCCO$</td>
<td>65% $VCCO$</td>
<td>$VCCO + 0.300$</td>
<td>0.45</td>
<td>$VCCO - 0.450$</td>
<td>7</td>
<td>-7.0</td>
</tr>
<tr>
<td>LVDCI 18</td>
<td>-0.300</td>
<td>35% $VCCO$</td>
<td>65% $VCCO$</td>
<td>$VCCO + 0.300$</td>
<td>0.45</td>
<td>$VCCO - 0.450$</td>
<td>7</td>
<td>-7.0</td>
</tr>
<tr>
<td>POD10</td>
<td>-0.300</td>
<td>$V_{REF} - 0.068$</td>
<td>$V_{REF} + 0.068$</td>
<td>$VCCO + 0.300$</td>
<td>See Tables 15 &amp; 16 in DS893</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>POD12</td>
<td>-0.300</td>
<td>$V_{REF} - 0.068$</td>
<td>$V_{REF} + 0.068$</td>
<td>$VCCO + 0.300$</td>
<td>See Tables 15 &amp; 16 in DS893</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSTL12</td>
<td>-0.300</td>
<td>$V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$VCCO + 0.300$</td>
<td>$VCCO/2 - 0.150$</td>
<td>$VCCO/2 + 0.150$</td>
<td>8</td>
<td>-8.0</td>
</tr>
<tr>
<td>SSTL135</td>
<td>-0.300</td>
<td>$V_{REF} - 0.090$</td>
<td>$V_{REF} + 0.090$</td>
<td>$VCCO + 0.300$</td>
<td>$VCCO/2 - 0.150$</td>
<td>$VCCO/2 + 0.150$</td>
<td>9</td>
<td>-9.0</td>
</tr>
<tr>
<td>SSTL15</td>
<td>-0.300</td>
<td>$V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$VCCO + 0.300$</td>
<td>$VCCO/2 - 0.175$</td>
<td>$VCCO/2 + 0.175$</td>
<td>10</td>
<td>-10.0</td>
</tr>
<tr>
<td>SSTL18 I</td>
<td>-0.300</td>
<td>$V_{REF} - 0.125$</td>
<td>$V_{REF} + 0.125$</td>
<td>$VCCO + 0.300$</td>
<td>$VCCO/2 - 0.470$</td>
<td>$VCCO/2 + 0.470$</td>
<td>7</td>
<td>-7.0</td>
</tr>
</tbody>
</table>

LVDS levels are defined in the following table.

Table 2 - LVDS Voltage Level Definition

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Common-Mode Voltage</td>
<td>+0.300V</td>
<td>+1.200V</td>
<td>+1.425V</td>
</tr>
<tr>
<td>Input $dV_{PP}$</td>
<td>100mV</td>
<td>350mV</td>
<td>600mV</td>
</tr>
<tr>
<td>Output Common-Mode Voltage</td>
<td>+1.000V</td>
<td>+1.250V</td>
<td>+1.425V</td>
</tr>
<tr>
<td>Output $dV_{PP}$</td>
<td>247mV</td>
<td>350mV</td>
<td>600mV</td>
</tr>
</tbody>
</table>

The motherboard shall implement selectable 100Ω differential termination on all Class 3 differential pin pairs. The motherboard shall provide selectable 50Ω “thevenin” termination for single-ended inputs and controlled-impedance drivers for single-ended outputs. These terminations are typically provided within the User FPGA on the motherboard. See Section 2.2.1.3 for an exception to the FPGA providing these terminations. The daughter board shall terminate motherboard outputs appropriately.

2.2.1.1 $V_{REF}$ Provision

By default, the $V_{REF}$ pin(s) of the FPGA on the motherboard shall be connected through a 500 ohm resistor to ground. This is intended for use with the Internal $V_{REF}$ feature of the Xilinx UltraScale FPGAs.

---

3 Taken from Tables 9 & 10 of Xilinx DS893, “Virtex UltraScale Architecture Data Sheet”, v1.0 dated July 10, 2014
4 Taken from Table 17 of Xilinx DS893, “Virtex UltraScale Architecture Data Sheet”, v1.0 dated July 10, 2014
5 $dV_{PP}$ is defined as ((P-N)-(N-P)) of the single-ended waveform. It is thus, by definition, the sum of the single-ended $V_{PP}$ values of the P and N signals.
As an alternative, a 2:1 reference voltage divider using the supplied VCCO and 1% resistors shall be provided. As another alternative, the mother board shall allow the SE1/VREF and SE3/VREF pins on the DNBC connector to be connected to the FPGA V_REF pin(s) using zero ohm resistors, allowing a daughter board to supply a more accurate or alternative reference voltage.

### 2.2.1.2 Power-On Sequencing Requirements Related to Class 3 Signals

See section 2.7.4.4.

#### 2.2.1.3 Differential Termination on Clock pins

The mother board shall provide an on-board 100Ω differential termination resistor on the B1S13P/B1S13N clock pair. This is required for example when implementing a memory interface running at +1.5V or below, while requiring the use of an LVDS clock to provide a reference frequency for the interface. No other pins shall have differential termination installed on the PCB by default, but other clock pins may include optional termination resistors. Daughter boards should be designed to expect this termination resistor to exist whenever possible.

The B1S13P/B1S13N SCK pair will have an external 100Ω resistor between them on the mother board that can only be removed by physically modifying the board. Do not use these pins for single-ended I/O (or in a pinch use only 1 of them). If they are used, a warning should be present in the user manual for the board.

### 2.2.2 Signal Routing Requirements

This section details routing requirements for Class 3 signals on the DNBC interface.

On the mother board, all signals shall be routed as 100Ω differential pairs / 50Ω single-ended signals. Loosely coupled routing is required. P to N length-matching must be done to within ±2.5 mils. All signals across the interface shall be length-matched to within 50 mils on the mother board. It is recommended that length-matching is done as closely as possible. Length-matching on the mother board shall account for the internal trace lengths within the FPGA device.

Routing constraints are especially tight for memory arrays implemented on daughter boards. The mother board shall meet the following constraints to insure DDR3 and DDR4 memory arrays will function at or near their maximum speeds (see Section 2.6 below):

- DMnx and DQxx to DQSpx/DQSnx - ±10 mils
- DMnx and DQxx (within each byte group) - ±7.5 mils
- DQSpx and DQSnx - ±2.5 mils
- DQSpx/DQSnx to DDR4A_CKp/n - -0.87”s to +10.5”
- Address/command/control - ±25 mils
- CKp/n - ±2.5 mils

To allow for length-matching on both the mother board and the daughter board, the above length-matching constraints for the mother board are one-half of the overall skew constraint, assigning the other half to the daughter board.

The daughter board has no specific signal routing requirements. Constraints for daughter board routing are application dependent and shall thus comply with any interface requirements, given the mother board routing mentioned earlier.

### 2.3 Interface Clocking Requirements

This section describes the clocking requirements for Class 3 signals on the DNBC interface.
For some mother boards (i.e., mother boards based on Virtex 6 and 7 FPGAs), there are two types of clocks on the interface, system clocks and local clocks. System clocks may be used to clock a synchronous interface across any (or all) banks on the DNBC interface with which they are associated. Local clocks may be used to clock signals within the bank only.

2.3.1 **Mother Board Clock Inputs**
There may be either one type of clock inputs on the mother board: global clocks; or there may be two types of clock inputs on the mother board: system clocks and local clocks.

The mother board shall accept a global or system clock on any of the system clock pairs defined in the pin map (Figure 1). A clock may be differential or single-ended; single-ended clocks shall use the ‘P’ component of the differential pair. Any signaling level accepted by Class 3 signals may be used.

The mother board shall accept a global or local clock on any of the local clock pairs defined in the pin map (Figure 1). A clock can be differential or single-ended; single-ended clocks shall use the ‘P’ component of the differential pair. Any signaling level accepted by Class 3 signals may be used.

2.3.2 **Clock Pin Selection**
When selecting system clock pins for use as inputs on the mother board, it is highly recommended that pair on pins (6, 5) is used first. When selecting local clock pins for use as inputs on the mother board, it is highly recommended that pair on pins (14, 13) is used first.

Since system clock pin inputs have a superset of local clock pin input functionality, it is highly recommended that, as a second-tier decision criteria relative to the above, system clock inputs be used in preference to local clock inputs.

2.4 **Cable Interface Requirements**
Any of the six connectors in a DNBC interface may be used for cabling to a DNBC interface connector on another FPGA on the same mother board or on another mother board. The standard cable is the HDR-180298-XX-SEAC from Samtec. This is a special version of the standard SEAC cable assembly. See Section 3.3 for further information.

With the standard signal mapping, the following connections are made between the two mother boards:

- TXxxp/n drives RXxxp/n and vice-versa
- SE0/VRP is connected to SE2 and vice-versa (by default SE0/VRP is not connected to the FPGA)
- SE1/VREF is connected to SE3/VREF and vice-versa
- VCCO is connected across the interface and the two connected systems must have the same VCCO voltage.
  - The two +12VDC pins are connected to the 12V_RTN pins and vice-versa
  - VCCO_SET is grounded at the local end of the cable
    - Both PWR_ON pins are connected to the PWR_ON pins at the remote system.
- VCCO is set to +1.86VDC when a cable is connected and only I/O standards compatible with +1.8V operation may be used.

2.5 **Daughter Board Interface Requirements**
As a minimum, a daughter board shall be installed on bank 0 of the DNBC interface. Depending on the required daughter board functionality, it can connect to only bank 0 (DNBC1), banks 0 and 1 (DNBC2), banks 0 to 2 (DNBC3) or to all six banks (DNBC6).

For each DNBC connector on a daughter board, the following resources are available:

- 52 I/O signals, consisting of 4 single-ended-only signals and 24 pairs, each of which may be used as a differential pair or as independent single-ended signals.
Four of the differential pairs may be used as clocks to the mother board.
+12VDC is available on 2 pins (1A maximum total per DNBC connector, 3A maximum across all three connectors) to power the daughter board.

Two VCCO pins are provided for the daughter board to power the I/O interfaces of the baseboard FPGA.

PWR_ON is provided to control and monitor daughter board power.
VCCO_SET may be used by low-power daughter boards to set the voltage of the VCCO regulator on the mother board to any valid supply voltage (see Section 2.7.6.4).

The mother board VCCO supply is normally set to +1.00VDC when a daughter board is installed, but may be overdriven by a VCCO supply on the daughter board, providing a reference supply voltage for the signals on that connector, as well as supplying power for I/O drivers and receivers on both the mother board and daughter board.

2.6 Memory Interface Requirements
The DNBC interface makes provision for memory interfaces to be implemented on top of the daughter board interface. To this end, byte groups are defined, so that a memory controller can be implemented on the main board that utilizes memory ICs or modules on the daughter board. There are some specific constraints that need to be adhered to when designing memory daughter boards that can be efficiently hosted by the main board.

2.6.1 Byte Group Pin Map
A pin map, denoting the byte groups in the DNBC interface, is given below. The four byte groups are two columns wide each and are separated by dotted lines.
## 2.6.2 Memory Interface Pin Assignments

The Xilinx UltraScale FPGAs have the most restrictive memory interface pin assignment rules and the DNBC interface has been designed to insure that it can be used with them. For FPGAs with less restrictive rules, there is more flexibility in connecting FPGA pins to interface pins on the mother board. UltraScale FPGAs have the following requirements for DDR3 and DDR4 memory interfaces (summary only, see the source document for complete rules)\(^6\):

- **Data Mask** - DM/DBI must be on the DM pin of the byte group
- **Data Strobe** - DQSp/n must be on the DQS pins of the byte group
- **Data** - The DQ pins must be used for the data bits of the byte group, in any order
- **Address and Control** - The UA and SE bits in a data byte group may be used for address and control functions. In non-data byte groups, all 13 pins may be used for address and control functions. All address and control pins must be in the same bank.
- **RESET** - reset_n can be on any pin as long as general interconnect timing is met and I/O standard can be accommodated for the chosen bank.
- **CLOCK** - The ck pair must be on one of the PN pairs in the Address/Control byte groups. Where there are multiple clocks, each should meet this requirement.
- **UNASSIGNED** - The Unassigned (UA) and Single-ended (SE) pins in each byte group may be used for any desired I/O signal compatible with the VCCO voltage required by the memory interface.

---

\(^6\) *UltraScale Architecture-Based FPGAs Memory Interface Solutions v6.1*, Xilinx PG150, dated November 19, 2014, pages 69 – 81.
2.6.3  **Data vs Control Pin Placement**
In general, data pins should be placed in banks 0 and 2. Control pins should be placed in bank 1. 

2.6.4  **Clock Placement**
If a reference clock is required, in general, it should be placed on system clock pair (6, 5) in bank 1. As discussed in Section 2.2.1.3, this differential pair has a termination resistor external to the FPGA on the mother board to insure proper termination when internal termination cannot be used.

2.6.5  **Routing Requirements**
Routing requirements vary between memory interface types. When a memory daughter board is designed, the requirements for the interface must be met, taking into account the routing that is guaranteed by the mother board (section 2.2.2).

2.7  **Power Provision & Control Signals**
This section details power delivery and system-level control signals on the DNBC interface.

Three power rails are available across the DNBC interface headers:  +12VDC for daughter board and sequencing power, $V_{CCO}$ for powering each interface bank and, for a cabled interface,  +12V_RTN for remote powering of the interface sequencing logic on the mother board.

The +12VDC rail is sourced from the mother board. The $V_{CCO}$ rail is split up into six isolated sub-rails, one per bank. Each of the $V_{CCO}$ rails may be provided by either the mother board or the daughter board.

Two power control signals are provided on the interface. The function of these signals is detailed in section 2.7.6.

2.7.1  **Hot Plugin**
The DNBC interface is not designed to support hot plugin of daughter boards and daughter boards should always be added and removed with the power off. Normally, cables cannot be connected and disconnected while system power is on. However, it is possible to modify the programming of the Configuration FPGA to implement a rudimentary form of hot plugin where power to the cable is turned off by the operator before connecting or disconnecting cables.

2.7.2  **+12VDC Power Rail**
The +12VDC power rail shall be driven by the mother board; it shall provide a voltage of $+12V \pm 10\%$. It is intended for use as an input voltage for switching power supplies on the daughter board. The mother board shall provide at least 3A on this rail and a daughter board shall draw no more than 3A from it.

Daughterboard power requirements above 3A shall be provided by an external power connection. For DNBC1 and DNBC2 daughter boards, a maximum of 1A and 2A of +12VDC current, respectively, may be drawn by the daughter board.

The mother board shall include a 5A fuse in-line with this supply to each DNBC interface. It is recommended that a 5A or greater fuse be installed in-line on the daughter board for this rail.

2.7.3  **+12VDC Power Return Rail**
To insure proper operation of all signals at a cabled DNBC interface, sequencing logic and circuitry for the interface shall be powered whenever the local system has +12V power or any system cabled across the interface is providing +12V power at the +12V_RTN pins. This is accomplished by using diodes to OR together these power supplies as the input voltage to the sequencing power regulator. This may be

---

7 Although this breaks interface encapsulation, best practices dictate that FPGA Design tools such as Xilinx Coregen Memory Interface Generator should be used to verify all planned memory interface pinouts for compatibility with main boards across the daughter card interface.
done across multiple DNBC interfaces. The sequencing power regulator shall draw no more than 30 mA from the +12V_RTN pins on any DNBC connector.

2.7.4 V\textsubscript{CCO} Rail
The V\textsubscript{CCO} rails are intended for use as a reference voltage for Class 3 signals, and as a source power supply for I/O buffers on Class 3 signals. The signals on each bank, B0-B5 are referenced to the corresponding V\textsubscript{CCO} voltage, and the voltage rails are to be isolated on the mother board (although not necessarily on the daughter board). The V\textsubscript{CCO} rails may be referred to as V\textsubscript{CCO,0} through V\textsubscript{CCO,5} for interface banks 0 through 5 respectively.

2.7.4.1 Cable Interface Requirements
The V\textsubscript{CCO} power rail is not used across a cabled DNBC interface connector, but are cross-connected across the cable. The connected V\textsubscript{CCO} power regulators must always supply the same (nominal) V\textsubscript{CCO} voltage so that the regulator on each mother board is used to power the local FPGA I/O buffers and minimal current flows across the cable. Each V\textsubscript{CCO} rail shall supply a minimum of 500mA of current at +1.8VDC for the local FPGA I/O buffers when cabled.

2.7.4.2 Daughter Board Interface Requirements
The voltage on the V\textsubscript{CCO} rail when a daughter board is installed shall be between +1.00VDC and +1.80VDC, nominal (+0.950VDC minimum to +1.890VDC maximum). The mother board shall provide power supplies that bias the V\textsubscript{CCO} rails to +1.00VDC ±5% when a daughter board is installed. These supplies shall provide a minimum of 500mA of current when the V\textsubscript{CCO} voltage is at +1.00VDC. The available current may increase at higher V\textsubscript{CCO} voltages. These supplies shall shut down without damage and shall sink no more than 20mA of current if a daughter board impresses a higher voltage on the V\textsubscript{CCO} rails.

The V\textsubscript{CCO} rails shall normally be driven by the daughter board and the biasing power supply on the mother board is not used to power a daughter board interface. For daughterboards whose V\textsubscript{CCO} power requirements are under 500mA total for both sides of the interface, the mother board biasing supply may be used to power both sides of the interface. In this case, the voltage of the mother board biasing supply may be modified from its nominal +1.00VDC level as explained in Section 2.7.6.4.

The daughter board shall normally provide at least 1A of current per interface bank, increasing to 2A if HSTL or SSTL signaling is to be used.

V\textsubscript{CCO} shall not come up faster than +12VDC.

2.7.4.3 V\textsubscript{CCO} Requirements for Banks with No Connected Pins
If a daughter board does not connect any of the pins within an entire I/O bank, it may leave V\textsubscript{CCO} for that bank unconnected. The mother board shall bias the V\textsubscript{CCO} rails on all unconnected connectors, including cabled connectors that are not connected to a remote system, to a voltage between +1.00VDC and +1.80VDC, nominal (+0.950VDC minimum to +1.890VDC maximum).

2.7.4.4 Power Sequencing Relative to V\textsubscript{CCO}
No Class 3 signal shall be driven above V\textsubscript{CCO}+ 0.3VDC by either mother board or daughter board. To meet this requirement it is recommended that both mother board and daughter board use V\textsubscript{CCO} as the V\textsubscript{CC} rail for their I/O buffers.

The daughter board must not drive V\textsubscript{CCO} power until the Power On (PWR_ON) signal has been asserted. See section 2.7.6.3 for an explanation of this.
2.7.5 **Ground Pins**

There are many ground pins on the DNBC interface headers. These serve both as digital ground (i.e. signal return paths and digital power supply grounds) and chassis ground. They shall be connected to digital ground on both mother and daughter boards.

2.7.6 **Control Signals**

There are two control signals on each connector at the DNBC interface, with PWR_ON connected to two opposing pins. These are used for power sequencing and interface management. Their purpose and associated requirements are described in this section.

2.7.6.1 **Usage**

The control signals at each interface connector are independent and are used to control power at that connector. The signals shall be isolated on the mother board, but not necessarily on the daughter board (i.e., the daughter board may use a single output to drive PWR_ON on multiple connectors on a single DNBC interface).

2.7.6.2 **Driver and Pull-Up Requirements**

The signals in this section specify the use of open-drain drivers and pull-ups. The requirements for these are specified below.

All open-drain drivers shall tolerate a voltage of up to +3.3VDC + 10% on their outputs, irrespective of the state of the board power rails. They shall be able to sink at least 4mA at a V_{OL} of +0.45VDC.

Except as noted, all input pull-ups shall be to a voltage of +1.80VDC ± 5%. They shall not provide current less than 100μA or in excess of 2mA when the signal they pull up is shorted to ground.

2.7.6.3 **Power On**

The PWR_ON signal, on both pin 110 and pin 112, is an active-high signal to indicate that the daughter board may power on its V_{CCO} power supplies. It is to be an open-drain output with a 1.00Kohm pullup on the mother board. Before this pin goes high, neither the mother board nor the daughter board may drive the V_{CCO} supplies or any of the I/O signal pins above ground.

A daughter board that requires an external power source for operation shall hold PWR_ON low using an open-drain driver until the external power is available and usable.

A daughter board may turn on internal power supplies before PWR_ON goes high or may turn on all power when it goes high.

For a cabled interface, PWR_ON indicates to the remote system that the mother board is ready to activate the bank interface by turning V_{CCO} on. Since the signal is on two cross-coupled pins, both systems drive the same signal line, which only goes high when both systems are ready to turn V_{CCO} on.

For both interfaces, the remote system or daughterboard must have V_{CCO} (and all other power supplies) stable and operational within 0.5 seconds after PWR_ON goes high.

2.7.6.4 **VCCO Voltage Set**

Pin 116 on each connector of the interface, VCCO_SET, controls the output voltage of the V_{CCO} bias regulator on the mother board.

For the cabled interface, VCCO_SET is a ground pin and is connected to the other ground pins at the local end of the cable. With this pin grounded, the V_{CCO} voltage is set to the maximum recommended V_{CCO} voltage for the FPGA - +1.86 ±0.03VDC.

Normally, with an installed daughterboard, the VCCO_SET pin is left floating and the V_{CCO} voltage is set to +1.00 ±0.03VDC while the daughterboard provides its own V_{CCO} power supply at a higher voltage.

---

8 Some feed-through on V_{CCO} is acceptable provided it does not exceed +0.7VDC.
However, daughterboards with limited \( V_{CCO} \) power requirements that can be supplied by the bias supply on the mother board may use the \( VCCO\_SET \) pin to modify the \( V_{CCO} \) supply voltage and not include their own supply. This is done by connecting a resistor between \( VCCO\_SET \) and ground. The resistor must be located next to the connector pin, with both ends routed using the shortest traces possible, to minimize noise pickup.

The mother board \( VCCO \) voltage is set as follows (approximately \( \pm 2\% \) tolerances on all voltages):

- \( VCCO\_SET \) open - \( V_{CCO} = +0.9995 \)VDC
- \( VCCO\_SET \) grounded - \( V_{CCO} = +1.8605 \)VDC
- \( VCCO\_SET \) grounded through a resistance \( R \) (KΩ) - \( V_{CCO} = (8.8488 + 4.528 \times R) / (4.756 + 4.53 \times R) \)

The mother board must use a TPS74201 1.5A Ultra-LDO from TI as the \( V_{CCO} \) regulator, or another regulator with the same output voltage set pin characteristics. The voltage set circuitry on the mother board shall be as shown in Figure 4. The threshold voltage at the set pin of the regulator is \( +0.800 \pm 0.004 \)VDC at \( T_J = 25^\circ \)C.

![Figure 4 – Mother Board VCCO_SET Circuitry](image)

### 2.8 DNBC Daughter Board Configuration Interface

This section describes the rules pertaining to Class 5 configuration signals on the DNBC interface, all of which are on a separate 14-pin header. The intent of these signals is to implement a serial configuration interface that can be used to program a daughter board-hosted FPGA from the mother board.

#### 2.8.1 Configuration Signal Interface

The Class 5 configuration signals form a sub-interface that is to a large extent independent from the rest of the DNBC interface. The only non-Class 5 signal that relates to Class 5 signals is PWR_ON. Pin assignments for the 14-pin, 2mm spacing DNBC Configuration header on the mother board (Molex 87831-1420 or equivalent) are shown below. A standard, 14-pin flat cable is used to connect this header to an identical header on a daughter board.
The below diagram describes the configuration interface, which is comprised of the Class 5 signals.

The DNBC configuration sub-interface is designed to be compatible with both Xilinx “Slave Serial” and Altera “Passive Serial” configuration modes. These modes are defined in Xilinx UG470 and the Altera Straitx-5 Handbook respectively.

All Class 5 signals are to be referenced to power supplies at +1.8V ±5%. Power supplies for the daughter board and for the mother board are intended to be separate. The daughter board power supply for the configuration signals is referred to as $V_{CCO\_CFG\_DC}$, the mother board power supply for the configuration signals is referred to as $V_{CCO\_CFG\_MB}$.

Signal function is described in section 2.8.2. Signal levels are defined in 2.8.2.6. Power-on interface function and power supply sequencing is described in section 2.8.4.

### 2.8.2 Signal Descriptions

This section describes the purpose and function of each of the Class 5 signals.

#### 2.8.2.1 PROG_B

The PROG_B signal is intended to be an active-low reset for the daughter board FPGA. PROG_B will be pulled to ground with a 10.0kΩ resistor on the main board. The daughter board will pull the PROG_B signal high to $V_{CCO\_CFG\_DC}$ with a 1.00KΩ resistor.

PROG_B is driven low or tri-stated by the mother board upon power-on. Once PWR_ON has been asserted, PROG_B will be tri-stated by the mother board. When the mother board initiates configuration, it shall pulse PROG_B low to clear the daughter board FPGA. PROG_B may never be driven high by the mother board, only tri-stated.
A daughter board not implementing the DNBC Configuration Interface may leave PROG_B floating or pull it low with a resistor.

2.8.2.2 INIT_B
The INIT_B signal is intended to be used as a signal, driven by the daughter board, that the daughter board is ready to accept configuration. When the INIT_B signal is high, the mother board may configure the daughter board. It shall be pulled low with a 10.0kΩ resistor on the main board. The daughter board will pull the INIT_B signal high to V_{CC_CFG_DC} with a 1.00KΩ resistor.

Daughter boards not implementing the DNBC Configuration Interface are recommended to connect the INIT_B signal to ground.

2.8.2.3 CCLK
The CCLK signal is the clock for the serial configuration data. The mother board shall transmit CCLK; the daughter board should use CCLK to clock in data from the DIN pin on the rising edge. The signal is driven with a 1.8V CMOS push-pull driver on the main board. It shall be pulled low with a 10.0kΩ resistor on the main board. It may be pulled low with a 1.00kΩ minimum resistor on the daughter board.

A daughter board not implementing the DNBC Configuration Interface may leave CCLK floating or pull it low with a resistor.

2.8.2.4 DIN
The DIN signal carries configuration data from the mother board to the daughter board. The mother board shall drive this signal with a 1.8V CMOS driver. It shall be pulled low with a 10.0kΩ resistor on the main board. It may be pulled low with a 1.00kΩ minimum resistor on the daughter board.

A daughter board not implementing the DNBC Configuration Interface may leave DIN floating or pull it low with a resistor.

2.8.2.5 DONE
The DONE signal is an active-high signal indicating that the daughter board FPGA has been configured successfully. It shall be pulled low with a 10.0kΩ resistor on the main board. It shall be either driven by the daughter board with a 1.8V CMOS driver, or pulled to V_{CC_CFG_DC} with a 1.00KΩ resistor and driven with an open-drain buffer.

A daughter board not implementing the DNBC Configuration Interface may leave DONE floating or pull it low with a resistor.

2.8.2.6 VREF
The VREF signal is a +1.80VDC reference voltage provided by the mother board. It shall be fused on the mother board and should only be used in conjunction with the configuration interface signals. Maximum load current on the daughter board shall be no more than 100 mA. This supply voltage is not necessarily synchronized with PWR_ON.

A daughter board not implementing the DNBC Configuration Interface may leave VREF floating.

2.8.3 Signal Levels and Standards
All configuration signals are to use LVCMOS18 levels (see Table 1 for exact levels). The V_{CC} power supply shall be +1.80V ±5% on both the mother board and the daughter board.

2.8.4 Power Sequencing
There are specific power-on sequencing requirements pertaining to the DNBC configuration sub-interface. Since the signals are powered by separate power supplies on the mother board and daughter board, care must be taken during power-on so as not to damage the mother board or daughter board.
On the mother board, no interface signals may be driven high until at least 0.5 seconds after PWR_ON has gone high. PROG_B must be held low while PWR_ON is off. The mother board should not assert PWR_ON until V_{CCO,CFG,MB} is within regulation.

The daughter board shall not power V_{CCO,CFG,DC} until PWR_ON is asserted. V_{CCO,CFG,DC} shall be within regulation within 0.5 seconds after PWR_ON is asserted.

The mother board shall not initiate configuration until the following conditions are met:

1. PWR_ON has been asserted and is high for at least 0.5 seconds
2. INIT_B is high (allowed to float by daughter board)
3. Mechanical Requirements
This section will describe the mechanical requirements for the DNBC interface. The mechanical requirements include specifying the Samtec SEAM/SEAF connectors used in the interface; describing the allowed mother board connector arrangements; describing the allowed daughter board outlines; and discussing system-level considerations.

3.1 Connector and Cable Specifications
The DNBC interface shall use the Samtec SEARAY series of connectors.

- The mother board shall use the **Samtec SEAF-30-05.0-L-04-2-A-LP-K-TR** connector. This connector includes latching posts at each end to retain a cable.
  - **Dini PID 4326**
- The daughter board shall use the **Samtec SEAM-30-07.0-L-04-2-A-K-TR** connector.
  - **Dini PID 4327**
- The cable shall be a modified **SEAC-030-04-15.7-TU-TU** cable, identified as **HDR-180298-01-SEAC**. The modification shall be in the mapping of signals between the two ends.
  - **Dini PID 4229**
- The Daughter Board Configuration Interface on both the mother and daughter boards shall be a **TE 5103308-2** or equivalent shrouded 2x7, 0.1" header.
  - **Dini PID 3887**

It is recommended that the mother board mount the SEAF connector on the solder side of the board. The daughter board shall always mount the SEAM connector on the solder side of the board. The daughter board shall have 4.0mm unplated holes in the circuit board at both ends of each SEAM connector to allow the latching posts of the main board SEAF to pass through the daughter board PCB.

![SEAM/SEAF Marketing Illustration](image)

*Figure 7 - SEAM/SEAF Marketing Illustration*
3.2 **Mother Board Connector Arrangements**

This section will detail the mother board connector arrangements designated for the DNBC interface. Two connector arrangements are allowed: one with the three cable-only connectors to the left of the three daughter board-allowed connectors (LEFT) and the other with them to the right (RIGHT), as shown in Figure 8 and Figure 9.

![Diagram of Mother Board Connector Arrangements](image-url)
The DNVUF1A, DNVUF2A, and DNVUF4A boards do not follow this numbering convention for the “RIGHT” DNBC arrangement, and therefore daughter cards plugging in to them will have mismatched numbering. Since the numbering is arbitrary, this mismatch can be ignored.
For both arrangements, the connectors and the mounting holes for standoffs to hold the daughter board are in specific patterns, so that a DNBC3 daughter board plus three connectors may be mounted at any DNBC interface. Daughter boards with all six connectors may be designed for use with either the LEFT (designated DNBC6L) or the RIGHT (designated DNBC6R) DNBC arrangement on a mother board. Adjacent DNBC interfaces connected to the same FPGA on a mother board shall be spaced 1mm between daughter boards (81mm between corresponding edges) to allow for a double-width daughter board.

3.3 **Cable Definition**

The standard cable used for the DNBC interface is the HDR-180298-01-SEAC, a modified version of the SEAC-030-04-15.7-TU-TU cable from Samtec. The cable has the following characteristics:

- 120-pin, 0.050” spacing, 50Ω single-ended coax jumper cable, using 50Ω, 36 AWG micro coax cable
- Cable length TBD
- Side latches for use with latch posts on the SEAF connector
- 60 signal pins and 60 ground pins

The cable provides cross-over signal mapping, as shown in Table 3.

### Table 3 - Cable Signal Mapping

<table>
<thead>
<tr>
<th>SIGNAL MAPPING</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>J1</strong></td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>9</td>
</tr>
<tr>
<td>13</td>
</tr>
<tr>
<td>17</td>
</tr>
<tr>
<td>21</td>
</tr>
<tr>
<td>25</td>
</tr>
<tr>
<td>29</td>
</tr>
<tr>
<td>33</td>
</tr>
<tr>
<td>37</td>
</tr>
<tr>
<td>41</td>
</tr>
<tr>
<td>45</td>
</tr>
<tr>
<td>49</td>
</tr>
<tr>
<td>53</td>
</tr>
<tr>
<td>57</td>
</tr>
<tr>
<td>61</td>
</tr>
<tr>
<td>65</td>
</tr>
<tr>
<td>69</td>
</tr>
<tr>
<td>73</td>
</tr>
<tr>
<td>77</td>
</tr>
<tr>
<td>81</td>
</tr>
<tr>
<td>85</td>
</tr>
<tr>
<td>89</td>
</tr>
<tr>
<td>93</td>
</tr>
<tr>
<td>97</td>
</tr>
<tr>
<td>101</td>
</tr>
<tr>
<td>105</td>
</tr>
<tr>
<td>109</td>
</tr>
<tr>
<td>113</td>
</tr>
<tr>
<td>117</td>
</tr>
</tbody>
</table>

**ALL GROUNDS COMMON AND TIED TO CABLE SHIELD**
3.4 Daughter Card Outline Definition

This section will detail the daughter card outlines designated for the DNBC interface. Five outline options are provided, differing only in the number of DNBC connectors provided: DNBC1 (52 interface signals), DNBC2 (104 interface signals), DNBC3 (156 interface signals), DNBC6L (312 interface signals, LEFT pattern) and DNBC6R (312 interface signals, RIGHT pattern). All daughter boards implementing the DNBC interface shall comply with one of these daughter board outlines. The default daughter board outline is the DNBC3, unless specific requirements exist to use one of the other sizes. All of the outlines are 168mm long and 80mm wide. The main body of the boards is 98mm long.

A daughter card implementing any outline option must cover the entire outline and implement all mounting holes, except as noted at the DNBC connectors. It is recommended that the mother board cover the entire daughter board outline and provide corresponding mounting holes. The mother board shall have matching mounting holes wherever the mother board overlaps a daughter board outline mounting hole.

Exceptions to the requirement to cover the entire outline may be made when an off-board connector placed on the daughter board requires a cut-out or “notch” in the side of the board. In this case the daughter board outline may be resized as appropriate.

The restricted component height limitation on the front of the board is provided to insure that adjacent cable connectors can be disconnected.

3.4.1 DNBC3 Daughter Board Outline

Figure 10 shows the DNBC3 daughter board outline. It is shown from the component side of the daughter card, with the DNBC connectors on the bottom side of the board. Where the main board overlaps the daughter board outline, the main board shall have the corresponding set of mounting holes to accept mother board to daughter board standoffs.
All dimensions in mm
The DNBC connectors are mounted on the solder side of the board and this view is through the PCB.

Figure 10 - Illustration of DNBC3 Daughter Card Outline

3.4.2 Alternate Daughter Board Outlines
Figure 11 shows alternate DNBC daughter board outlines. The DNBC1 and DNBC2 outlines narrow the connector neck to cover just one or two connectors, as shown. All daughter boards must include
connector 1. The DNBC6 daughter boards widen the connector neck to include connectors 4 through 6, either on the right (as shown) for DNBC6R or on the left for DNBC6L. The extension is 1mm shorter than the neck on the other side, to allow another DNBC daughter board next to this one. The connectors not used for the DNBC1 and DNBC2 daughter boards are available for cabling.

![Figure 11 - Illustration of Alternate DNBC Daughter Card Outlines](image)

3.4.3 Double-Width Layout Outline
A double-width layout outline may be allowed for on a system level. Requirements for this outline are specified in section 3.7.3.

3.4.4 Example Daughter Board Layouts
This section features some example DNBC3 daughter board layouts. This section does not contain any recommendations or requirements; it exists solely to illustrate how the DNBC interface daughter board outlines may be adapted for common use cases.
3.5 Daughter Board Configuration Interface Description

The Configuration Interface for DNBC daughter boards shall use identical 14-pin headers on both boards, joined by a 14-wire ribbon cable. The mother board shall include one or more (for example, one per User FPGA) Configuration headers, located for cabling to all DNBC interface positions. A DNBC daughter board only requires the interface if it includes an FPGA that is to be included in the mother board configuration string.

The Configuration header is a 14-pin, 2mm shrouded header, Molex part number 87832-1420 (PID 511). The ribbon cable is a 14 conductor, 1.0 mm centers Round Conductor Flat Cable, 28AWG (7 x 36) stranded copper conductors; gray PVC with pin #1 edge marked. Available configuration cables include a 12” cable (PID 1333) and a 40” cable (PID 4395).
3.6 **Daughter Board Mezzanine Stack Description**

This section will describe the mezzanine stack for DNBC daughter boards. Included will be a specification for the hardware used, spacing requirements and drawings for mated connector systems.

3.6.1 **Mounting Hole Coverage and Attachment**

All mounting holes in each outline shall be used to secure the daughter board and mother board together. If the mother board does not cover the extent of some of the daughter board outline and (necessarily) lacks the appropriate mounting holes, adequate support for the daughter board must be provided.

The daughter board must always fill the entire outline and hence shall implement all mounting holes called out in this specification. See section 3.1 for more information about daughter board outlines and mounting hole locations.

3.6.2 **Stack Illustration**

The DNBC interface specification assumes that the SEAF connector is mounted on the top side of the mother board and the SEAM connector on the solder side of the daughter board. The DNBC interface stack assumes no baseplate directly on the back side of the mother board. The stack for all DNBC interfaces is illustrated below:

![Illustration of Stack for all DNBC Applications](image)

**Figure 13 - Illustration of Stack for all DNBC Applications**

This section will detail the mechanical requirements of the DNBC interface with regards to the mezzanine-style stacking orientation.

3.6.2.1 **Clearance Requirements**

The main board shall have top side components (between the main board and daughter board) no taller than 5.35mm where the daughter board outline overlaps the main board. The main board is recommended to have a thickness of 0.100".

The daughter board shall have backside components (between the daughter board and the mother board) no taller than 4.00mm. The daughter board is recommended to have a thickness of 0.062". The DNBC interface makes no recommendations for component side component heights for daughter boards in non-chassis applications, except for the areas with restricted component heights that are provided to insure that adjacent cable connectors can be disconnected.

It is recommended that the top surface of any components taller than 2mm between the two boards be either electrically insulated or shorted to digital ground.

3.6.2.2 **Hardware Requirements**

It is required that the mainboard is attached to the daughter board using five 4.5mm hex, 12mm” long, female-female, M3-threaded standoffs. It is recommended that these standoffs be stainless-steel.

It is required that the main board and the daughter board be attached to the standoffs using 6mm long screws, threaded with M3 threads. It is recommended that they be Phillips-head screws made of alloy steel with zinc plating.

Suggested stack mounting hardware:
3.6.2.3 Mechanical Assembly Illustration
The following is a mechanical assembly illustration for the standoff and board mezzanine stack.

![Mechanical Assembly Illustration](image)

Assembled Stack
Recommended order of assembly:
1. Mother Board PCB to standoff
2. Daughter board PCB to standoff

3.7 Chassis and System-Level Requirements for DNBC Implementations
This section will describe chassis and system requirements for boards implementing the DNBC interface. In particular, the location of the chassis rear panel and connector placement guidelines will be described. Power dissipation requirements will also be addressed.

3.7.1 Daughter Board Component Height Limitation
In section 3.6.2.1 we defined the daughter card solder side component height limitations. The daughter board component side height limit shall be 27mm. It is recommended that any components taller than 4mm have their tops be either insulated or shorted to digital ground.

3.7.2 Daughter Board Spacing
Adjacent daughter board positions on the same FPGA shall be spaced at exactly 81mm center to center.

3.7.3 Double-Wide Daughter Boards
Two adjacent mother board positions on the same FPGA may be occupied by a single “double wide” daughter board, as shown in Figure 15.

Physically, the daughter board shall assume spacing as defined in 3.7.2 and shall take up the outlines of both boards, including the space between the two positions. All mounting holes within both outlines will be implemented.

Electrically, the daughter board will treat the two DNBC connectors as separate interfaces. The +12VDC power rails shall remain isolated; the daughter board may not connect them together. All control signals must be implemented independently. $V_{CCO}$ rails may be connected together on the daughter board; in this case, the daughter board must wait for both interfaces to assert PWR_ON before bringing up $V_{CCO}$. The double-wide daughter board must not make any assumptions regarding the behavior of the power rails on one interface relative to the other.
For double-wide daughter boards, it is required that electrical resources on the left DNBC Interface are used first, before using resources on the right Interface. Unused electrical resources (unconnected power rails or signals) should be dealt with in accordance to the rules laid out in section 2.1.1.5.

### 3.7.4 Daughter Board Cabling

External connections to a DNBC daughterboard shall be made at the top edge of the board or using vertical connectors on the component side of the board. No connections shall be made along the sides of the board. DNBC daughter boards on opposite sides of a mother board should be separated so as to provide a cabling trough between the daughter boards, as shown below.
3.7.5 **Power Dissipation**
The system design shall make provision for the daughter card to dissipate the maximum rated power that the DNBC interface provides via the Class 1 Power pins (section 2.7). Any additional power dissipation on the card, made possible (for example) through an external power header, is not accounted for by the system-level provisions of the DNBC specification.

The chassis shall provide an ambient air temperature of no warmer than 50°C. There is no minimum chassis airflow guaranteed for the DNBC daughter board.

3.7.6 **Daughter Board Power Monitoring**
Within space constraints, DNBC daughterboards shall provide a green LED to indicate that +12VDC power is available (in case the fuse on the mother board is blown) and one red LED for each power supply to indicate that it is not within approximately ±5% of its nominal value. Within space constraints, DNBC daughterboards shall use a window comparator for each supply, checking for both undervoltage and overvoltage conditions.
Appendix A. Design Check Lists
This section provides check lists to help validate mother board and daughter board designs.

A.1. Mother Board Check List

☐ An external 100 ohm termination resistor is used on the B1S13P/B1S13N signal pair to provide clock termination at VCCO voltages other than +1.8VDC.

☐ The VRP pins in all banks on the FPGA connected to DNBC connectors are connected as follows: 240 ohm termination resistor to ground and a DNI resistor to the SE0/VRP pin on the connector.

☐ The VREF pins in all banks on the FPGA connected to DNBC connectors are connected as follows: 499 ohm termination resistor to ground; DNI resistor to VCCO to provide a voltage divider; and DNI resistors to the SE1/VREF and SE3/VREF pins on the connector.

☐ All pins on all DNBC connectors are connected as specified. If there have to be exceptions, a warning is included in the User’s Manual.

☐ Consecutive FPGA banks are connected to the first three DNBC connectors and memory controllers may be configured for a daughter board.

☐ All Class 3 signals are connected to the proper FPGA I/O pins, meeting the required signaling standards and VCCO voltage range.

☐ All Class 3 interface signals are routed as loosely coupled 100 ohm differential pairs or (for the Sex signals) as 50 ohm single-ended traces, meeting all of the length-matching requirements. Internal FPGA lengths are included as part of the length-matching.

☐ The defined input clock pins at the connector are connected to appropriate clock input pins on the FPGA.

☐ The signals within each memory byte group are connected correctly to the FPGA, so that daughter boards implementing memory arrays will function properly. Pin assignments should be verified by implementing a memory controller in the FPGA.

☐ The +12VDC rail to each DNBC interface includes a series fuse and can provide up to 3A to a daughter board.

☐ The sequencing logic for the DNBC interface is powered by the local +12V supply or the +12V_RTN power pins.

☐ The VCCO bias supply is turned off unless PWR_ON for the DNBC interface is high or the connector is totally unconnected. When a cable is installed, a minimum of 500mA of current at +1.8VDC is available for FPGA I/O buffers. When a daughter board is installed, the bias voltage shall be +1.00VDC.

☐ The VCCO bias supply shuts down (or draws some minimal current) when a higher VCCO voltage is provided by a daughter board, up to +1.89VDC.
PWR_ON is connected to both pins on each DNBC connector, using an open-drain driver (+3.3VDC maximum) with a 1.00K pullup resistor. The daughter board or cabled system can pull PWR_ON low.

The VCCO bias supply is located close to the VCCO_SET pin and has the proper resistor network at this pin to set the VCCO bias voltage as defined.

At least one DNBC Daughter Board Configuration Interface header is provided and properly connected to the Configuration FPGA.

The physical placement of the six connectors in each DNBC interface match either the LEFT or RIGHT placement pattern.

Each DNBC interface position provides clearance for a DNBC3 daughter board or for six cables, without interference from other components or the chassis.

All specified mounting holes are provided at each DNBC interface.

Top side components under the DNBC3 daughter board outline are less than 5.35mm tall.

Adjacent DNTC interfaces on the same FPGA are spaced properly for double-wide daughter boards.

Adequate space is provided at the top end of the DNBC daughter boards for cabling.

### A.2. Daughter Board Check List

- A differential pair consistent with the external 100 ohm termination resistor is connected to the B1S13P/B1S13N signal pair or only a single single-ended signal is connected to one of these pins. If two single-ended signals must be connected, as a last resort, a warning is included in the User’s Manual to delete the termination resistor on the mother board.

- If a non-standard VRP termination is required or the SE0/VRP pin on a connector must be used as SE0, a warning is included in the User’s Manual to delete the termination resistor on the mother board and connect the connector pin.

- If a VREF signal from a daughter board is required, a warning is included in the User’s Manual to connect the VREF pin on the mother board FPGA to the SE1/VREF or SE3/VREF pin on the connector.

- All interface signals are used appropriately, meeting the VCCO voltage range requirements and using available signaling standards.

- All interface signals are routed appropriately, based on their usage and with length-matching based on their maximum required frequencies.

- Clock inputs are connected to the defined clock pins on the DNBC connectors.

- If a memory array is implemented, all byte group pins are connected correctly. Pin assignments should be verified by implementing a memory controller in the FPGA.
The daughter board draws no more than 3A from the +12VDC supply. If additional power is required, external connectors are provided.

The daughter board either has its own VCCO supply (+1.0VDC minimum to +1.8VDC maximum) or draws no more than 500mA from the mother board’s bias supply.

The daughter board does not turn on VCCO until PWR_ON is high. VCCO is stable and operational within 0.5 seconds after PWR_ON goes high.

The circuitry, if any, at the VCCO_SET pin is located close to the pin to minimize noise pickup and is designed to set the required VCCO voltage(s).

If the daughter board includes an FPGA, a DNBC Daughter Board Configuration Interface header is provided and properly connected to the FPGA.

The daughter board meets the appropriate outline, including all mounting holes. The clearance holes at both ends of the DNBC connectors are included.

The three DNBC connectors are in the correct order.

Back side components (except for the DNBC connectors) are less than 4.00mm tall.

All daughter board cabling is at the top end of the board or uses vertical connectors.

The daughter board includes a green LED for the +12VDC supply and red fault LEDs for the local power supplies, preferably using window comparators.