DNTEC

Dini Transceiver Connection

Interface Specification

Revision 1.4

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Dini Group, Inc.

Last Updated 2017-11-15, N. Harder
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1 Overview
This document describes the DNTC (Dini Transceiver Connection) expansion interface. Mechanically, the DNTC interface consists of a single 320-pin connector on a mother board that has the following characteristics:

- Sixteen high-speed transceiver lanes connected to a User FPGA on the mother board, divided into four four-lane blocks.
- 32 out-of-band GPIO signals connected to the User FPGA and usable as differential pairs and/or single-ended signals.
- Four differential transmit reference clocks from the mother board plus four differential receive reference clocks to the User FPGA, each associated with a transceiver block.
- A low-speed serial management bus that can also be used as an FPGA programming interface.
- Power sequencing and control signals.

The goal of the DNTC interface is to specify a flexible and modular expansion interface that can be used to augment the functionality of off-the-shelf Dini Group ASIC Emulation systems. The principal use model is to customize features and interfaces available on a Dini Group ASIC emulation mother board, which itself hosts one or more FPGAs, with transceiver interfaces such as PCI Express (GEN1 – GEN3), SATA (Rev 1 – Rev 3), 10Gbps Ethernet and similar interfaces with up to 16Gbps data rates. Thus, the ASIC emulation system can be tailored to support an end-user’s desired feature mix.

The DNTC interface includes two standard daughter board physical outlines and custom alternatives include combined DNTC-DNBC (Dini Bank Connector Interface) daughter boards. Section 3.1 describes the physical outline options.

The DNTC interface is primarily intended to be used on Dini Group Xilinx UltraScale ASIC emulation products, but can also be used on Altera baseboards or retrofitted onto baseboards with older Xilinx technologies. It is not backwards compatible with the Dini Group DNSEAM or DNIOB transceiver expansion interfaces such as that found on the Dini Group Virtex-7 and older ASIC emulators.

1.1 Other Files
This specification makes reference to several files and drawings. They are enumerated here:

1. DNTC Mechanical.vsd – an annotated set of drawings describing the DNTC daughter board form factor.

1.2 Terminology & Style
A variety of terminology is used throughout this document. Some of it has very specific meaning.

The phrases **are to/shall/required/must** state hard requirements for all cards implementing the DNTC interface. The words **highly recommended** denote characteristics that are not hard requirements, but should be implemented where possible and **are likely to become requirements in future major revisions**.
of the DNTC specification. The word recommended denotes characteristics that are not hard requirements nor likely to become such, but should be implemented where reasonable.

The terms “mother board,” “main board,” “baseboard” and “host” are used interchangeably, and refer to the FPGA-based Dini Group ASIC emulation board. The term “daughter board” refers to the smaller mezzanine-mounted expansion board.

The phrases “DNTC Interface” and “DNTC Slot” are used interchangeably to refer to each DNTC connector pattern on a mother board.

1.3 Revision History

0.1 – 2015-02-26, A. Sikes
1. Initial Revision

0.2 – 2015-03-06, A. Sikes
1. VCCO voltage changed to +1.2V thru 3.3V.
2. VCCO_SET definition in section 2.6.6 changed to allow setting between +1.224VDC and 3.000VDC.
3. Table 3 modified to agree with 3.3V-capable interfaces.
4. Section 3.4.4 added.
5. Numerous editorial changes and clarifications made.

0.3 – 2015-04-09, A. Sikes
1. Changed document type from pdf to vsd in Section 1.1.
2. Section 2.1.1.6: Change OOB signals to loosely-coupled.
3. Section 2.1.1.7: Include use for FPGA Configuration.
4. Section 2.4.2.1: Added requirement to drive both VREF pins.
5. Section 2.4.4: Added boxed warning about needing to change mother board resistors to use PCIe hard-wired resets.
6. Reordered sections of 2.5 to have Managed versus Unmanaged first. Split Management Bus Timing into a separate section, 2.5.5.
7. Added second warning box about needing to reduce the +1.35VDC bias voltage in some cases.
   Redid Figure 5.
8. Section 3.2: Clarified drawings to show Interface Connector locations.
9. Various minor changes to correct grammar.

0.4 – 2015-04-10, A. Sikes
1. In Figure 1, changed pin 5 from RSVD to PRSNT2#.
2. In Figure 2, added the PRSNT2# pin and deleted RSVD_0.
3. Expanded Section 2.6.2 to add PRSNT2# and added Table 6.

0.5 – 2015-04-11, A. Sikes
1. Changed Table 6 to include “Not Used” as a separate entry.
0.6 – 2015-04-21, A. Sikes
1. Moved PRSNT# from pin 5 to share pin 298 with INT#.
2. Figures 1 and 2 modified to show new location of PRSNT2#.
3. Sections 2.5.4.3 and 2.6.2 modified to describe the sharing.

0.7 – 2015-05-22, A. Sikes
1. Added a comment on the allowed OOB signal levels in Section 2.4.
2. Added recommendation in Section 2.4.1 to group related OOB signals in the TX or RX bank rather than by TX/RX pairs.
3. Expanded Section 3.4.4 to include the +3.3VDC supply and to indicate why it helps to have LEDs on the +12/3.3VDC supplies.
4. Added Appendix A, Design Check Lists.

0.8 – 2015-07-15, A. Sikes
1. Changed PWR_ON in Section 2.6.3 to require a pullup on the mother board and not on the daughter board.

1.0 – 2015-10-21, A. Sikes
1. Modified Figure 11 and Section 3.3.2.2 to use M3 hardware for the stack rather than 4-40.

1.1 – 2016-03-17, A. Sikes
1. Modified Sections 3.3.2.2 and 3.3.2.3 to recommend Phillips-head screws rather than Allen-head screws and to delete the washers.

1.2 – 2016-06-22, A. Sikes
1. Modified Sections 3.2.3 and Figure 9 to recommend the RIGHT outline and to add dimensions for DNTBC3 boards.

1.3 – 2016-08-26, A. Sikes
1. Sections 3.2 and 3.3.2.1 modified to indicate the reason for height restrictions along the sides of the board.

1.4 – 2017-11-15, A. Sikes
1. Figure 7 and Figure 8 in Section 3.2 updated to show the alignment pins in the correct locations.

1.4 Contact
For questions or comments regarding the interface specification, contact support@dinigroup.com.
# Electrical Requirements

This section will define electrical requirements for the DNTC interface. Enumerated will be requirements for signals, including signaling standards and routing requirements, as well as description of the logical interface requirements such as synchronous I/O timing information. Also in this section non-signal electrical requirements, i.e. power distribution, will be described.

## 2.1 Signal and Pinout Description

This section will describe the signals and pinout for the DNTC connector.

A pinout of the DNTC interface connector is given below. Pin numbers follow the SEAM/SEAF pin numbering convention. All pin numbers with “P” or “p” represent the true component of a differential signal. All pin numbers with “N” or “n” represent the complementary component of a differential signal.
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The figure below shows the schematic symbol for the DNTC mother board header (nominally a Samtec SEAF-40-05.0-L-08-2-A-K-TR connector, see section 3.1). The daughter board header symbol is identical. Some annotation within the symbol is provided; this annotation will be clarified later in this document.
2.1.1 Signal Class Definitions

This section will group the DNTC interface signals into signal classes. The following sections define the functionality and characteristics of each of the classes, and define terminology associated with them.

2.1.1.1 Class 1 – Ground
All ground pins are class 1 pins. These are both digital ground and chassis ground. See section 2.7.1.

2.1.1.2 Class 2 – Power
The Power pins include +12VDC, +3.3VDC and VCCO. See section 2.7.

2.1.1.3 Class 3 – Control and Reserved
The Control pins are responsible for power sequencing and card detection. The control pins are PRSNT#, PRSNT2#, PWR_ON, PWR_GD, HW_RST# and VCCO_SET. The Reserved pins are not currently used and are available for future use. See section 2.6.

2.1.1.4 Class 4 – Transceiver Lanes
These differential pairs form the multi-gigabit SERDES links between the FPGA on the main board and the DNTC daughter board. Each of the sixteen transceiver lanes consists of a transmit differential pair from the mother board to the daughter board, labeled “TX”, and a receive differential pair in the reverse direction, labeled “RX”. The transceiver lanes are divided into four banks, labeled “B0” through “B3.” See section 2.2 for additional information.
2.1.1.5 Class 5 – Reference Clocks
The four transmit reference clocks (B0_TREFCLKp/n through B3_TREFCLKp/n) are each a differential pair generated by a low-jitter clock generator on the mother board for use on the daughter board. Each of the four receive reference clock differential pairs (B0_RREFCLKp/n through B3_RREFCLKp/n) is an AC-coupled differential pair on the mother board to the transceiver reference clock input for the corresponding bank of transceivers at the FPGA. See section 2.3.

2.1.1.6 Class 6 – Out-of-Band I/O Signals
These 32 pins are used for general-purpose digital signaling between the mother board and the daughterboard. They are routed as loosely-coupled differential pairs on the main board, but can also be used single-ended at reduced frequencies. See section 2.4.

2.1.1.7 Class 7 – Management Bus
The Management Bus is generally only used for managed daughter boards (see Section 2.5.1 for details). It implements an “enhanced” 4-wire SPI-type serial bus connection between the Configuration FPGA on the main board and a CPLD on the daughter board. The bus signals and the rules governing their functionality are described in Section 2.5. Alternatively, based on reprogramming of the Configuration FPGA on the baseboard, these signals may be used for configuration of FPGAs on daughter boards (see Section 2.5.6).

2.1.2 General Signal Connection Requirements
The mother board shall have all of the interface signals connected appropriately, such that all signals function as defined. The daughter board is not required to connect all of the class 4, 5, 6 or 7 signals. Unconnected signals shall be left floating, except that unused transceiver receive inputs should be grounded. All class 1, 2 and 3 signals must be implemented in accordance with sections 2.6 and 2.7.

2.1.3 General Signal Routing Requirements
Due to the high frequencies encountered with transceiver signals (data rates to 16 Gbps), a low-loss dielectric material (Isola FR408HR or similar) shall be used throughout the mother board stackup to reduce signal attenuation at high frequencies. A similar low-loss material is also recommended for the daughter board, if it implements transceiver channel connections.

2.2 Class 4 Transceiver Signals
This section defines the signaling standards to be employed, signaling levels to be tolerated, and physical routing requirements for the class 4 transceiver signals. These differential pairs form the multi-gigabit SERDES links between the main board and the daughter board. They are DC-coupled between the DNTC connector and the transceiver pins on the User FPGA.

2.2.1 Transceiver Bank Assignments
Xilinx FPGAs have four transceiver lanes per bank while Altera FPGAs have six lanes per bank. On a Xilinx-based mother board, each DNTC transceiver bank shall be connected to a single FPGA transceiver bank. On an Altera-based mother board:
• DNCTC transceiver banks B0 through B2 shall each be connected to a single FPGA transceiver bank.
• DNCTC transceiver bank B3 can either be connected to a single FPGA transceiver bank or can be connected to the unused lanes in the FPGA banks used for DNCTC banks B0 and B1.

Lane assignments within each bank shall be made such that for a PCI Express interface, DNCTC lanes 0 through 3 correspond to PCIe lanes 0 through 3.

2.2.2 Transceiver Bonding Requirements
On the motherboard, all eight lanes in banks B0 and B1 shall have the capability of being bonded. It is recommended that that the eight lanes in banks B2 and B3 also have the capability of being bonded, if possible.

2.2.3 Signaling Standards and Termination for Class 4 Signals
This section defines the signaling standards applicable to the class 4 transceiver signals and the specific electrical characteristics of the transmitters and receivers. Electrical characteristics differ somewhat between Xilinx and Altera FPGA transceivers and daughter boards shall be designed to function properly with both.

The following table summarizes the DC characteristics of the Xilinx UltraScale GTH transceiver.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>DC Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVPPIN</td>
<td>Differential peak-to-peak input voltage (external AC coupled)</td>
<td>&gt;10.3125 Gb/s</td>
<td>150</td>
<td>–</td>
<td>1250</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.6 Gb/s to 10.3125 Gb/s</td>
<td>150</td>
<td>–</td>
<td>1250</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 6.6 Gb/s</td>
<td>150</td>
<td>–</td>
<td>2000</td>
<td>mV</td>
</tr>
<tr>
<td>VIN</td>
<td>Single-ended input voltage. Voltage measured at the pin referenced to GND.</td>
<td>DC coupled ( V_{\text{MGTAVTT}} = 1.2 \text{V} )</td>
<td>-400</td>
<td>–</td>
<td>(V_{\text{MGTAVCC}})</td>
<td>mV</td>
</tr>
<tr>
<td>VCMIN</td>
<td>Common mode input voltage</td>
<td>DC coupled ( V_{\text{MGTAVTT}} = 1.2 \text{V} )</td>
<td>–</td>
<td>2/3 (V_{\text{MGTAVTT}})</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>DVPPOUT</td>
<td>Differential peak-to-peak output voltage(^2)</td>
<td>Transmitter output swing is set to 1010</td>
<td>800</td>
<td>–</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>VCMOUTDC</td>
<td>Common mode output voltage: DC coupled</td>
<td>Equation based ( V_{\text{MGTAVTT}} - \frac{D_{\text{VPPOUT}}}{4} )</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>VCMOUTAC</td>
<td>Common mode output voltage: AC coupled</td>
<td>Equation based ( V_{\text{MGTAVTT}} - \frac{D_{\text{VPPOUT}}}{2} )</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Rin</td>
<td>Differential input resistance</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>–</td>
<td>Ω</td>
</tr>
<tr>
<td>Rout</td>
<td>Differential output resistance</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>–</td>
<td>Ω</td>
</tr>
<tr>
<td>TOSKEW</td>
<td>Transmitter output pair (TXP and TXN) intra-pair skew</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>Ps</td>
</tr>
<tr>
<td>CEXT</td>
<td>Recommended external AC coupling capacitor(^3)</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>–</td>
<td>nF</td>
</tr>
</tbody>
</table>

\(^1\) Taken from Table 41 of Xilinx DS893, "Virtex UltraScale Architecture Data Sheet", v1.0 dated July 10, 2014
\(^2\) The output swing and pre-emphasis levels are programmable using the attributes discussed in the UltraScale Architecture GTH Transceiver User Guide (UG576), and can result in values lower than reported in this table.
\(^3\) Other values can be used as appropriate to conform to specific protocols and standards.
The following table summarizes the DC characteristics of the Altera Stratix V GX/GS transceiver.

### Table 2 – Stratix V GX/GS Transceiver DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>DC Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(DV_{\text{PPIN}})</td>
<td>Differential peak-to-peak input voltage (external AC coupled)</td>
<td>(V_{\text{CCR,GXB}} = 1.0V (V_{\text{ICM}} = 0.75V))</td>
<td>85</td>
<td>–</td>
<td>1800</td>
<td>mV</td>
</tr>
<tr>
<td>(DV_{\text{PPIN}})</td>
<td>Differential peak-to-peak input voltage (external AC coupled)</td>
<td>(V_{\text{CCR,GXB}} = 0.90V (V_{\text{ICM}} = 0.6V))</td>
<td>85</td>
<td>–</td>
<td>2400</td>
<td>mV</td>
</tr>
<tr>
<td>(DV_{\text{PPIN}})</td>
<td>Differential peak-to-peak input voltage (external AC coupled)</td>
<td>(V_{\text{CCR,GXB}} = 0.85V (V_{\text{ICM}} = 0.6V))</td>
<td>85</td>
<td>–</td>
<td>2400</td>
<td>mV</td>
</tr>
<tr>
<td>(V_{\text{IN}})</td>
<td>Single-ended input voltage. Voltage measured at the pin referenced to GND.</td>
<td>DC coupled</td>
<td>-400</td>
<td>–</td>
<td>1200</td>
<td>mV</td>
</tr>
<tr>
<td>(V_{\text{ICM}})</td>
<td>Common mode input voltage</td>
<td>AC and DC coupled</td>
<td>–</td>
<td>600/700/750</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>(V_{\text{OD}})</td>
<td>Differential peak-to-peak output voltage</td>
<td>(V_{\text{OD setting}} = 63)</td>
<td>–</td>
<td>1260</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>(V_{\text{OCMDC}})</td>
<td>Common mode output voltage</td>
<td>DC coupled</td>
<td>–</td>
<td>650</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>(V_{\text{OCMAC}})</td>
<td>Common mode output voltage</td>
<td>AC coupled</td>
<td>–</td>
<td>650</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>(R_{\text{IN}})</td>
<td>Differential input resistance</td>
<td>–</td>
<td>85/100/120/150</td>
<td>–</td>
<td>(\Omega)</td>
<td></td>
</tr>
<tr>
<td>(R_{\text{OUT}})</td>
<td>Differential output resistance</td>
<td>–</td>
<td>85/100/120/150</td>
<td>–</td>
<td>(\Omega)</td>
<td></td>
</tr>
</tbody>
</table>

Receive inputs to the mother board are DC-coupled and shall tolerate single-ended \(V_{\text{IN}}\) between -0.40\(V_{\text{DC}}\) and +1.00\(V_{\text{DC}}\). The input differential swing shall be at least 150 mV minimum. The maximum differential swing shall be 1250 mV above 6.6Gbps and 2000 mV below 6.6Gbps. The typical receiver common mode input voltage shall be between 600 mV and 800 mV.

Transmit outputs from the mother board are DC-coupled. The output differential swing shall be configurable between at least 300 mV and 1100 mV, nominal.

The mother board shall implement selectable 100\(\Omega\) differential termination on all transceiver differential pin pairs. Daughter boards shall use AC-coupling and/or DC-biasing networks to meet the voltage limits and common mode voltage requirements of the mother board.

#### 2.2.4 Transceiver Signal Routing Requirements

This section details routing requirements for the class 4 transceiver signals at the DNTC interface.

On the mother board, all signals shall be routed as 100\(\Omega\) differential pairs from the signal source to a single load device. These differential pairs shall be routed on separate stripline layers within the main board, using GSG stacking for increased signal isolation, and 5-mil trace width to reduce skin loss. Receive and transmit pairs shall be routed on separate layers to increase RX-TX isolation. Tightly coupled routing is required. P-to-N length-matching must be done to within 10 mils. It is recommended that length-matching is done as closely as possible. Length-matching on the mother board shall account for the internal trace lengths within the FPGA device. Similar routing requirements are highly recommended for daughter boards.

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4 Taken from Table 41 of Xilinx DS893, “Virtex UltraScale Architecture Data Sheet”, v1.0 dated July 10, 2014

5 The output swing and pre-emphasis levels are programmable using the attributes discussed in the Altera Transceiver PHY IP Core User Guide (UG-01080), and can result in values lower than reported in this table.
There shall be no more than 500 mils of skew between all group 4 signals on the mother board.

This interface specification does not define a maximum trace length for group 4 signals. However, it is highly recommended that trace lengths be kept as short as reasonably possible on both the mother and daughter boards.

**Design note:** If AC-coupling is required on the SERDES channels for a particular design, the AC coupling capacitors must be implemented on the daughter board.

**Recommendation:** Daughter boards should use a low-loss dielectric material if the SERDES channels are run at multi-Gigabit speeds.

Both mother boards and daughter boards shall use high-frequency design techniques to maximize the achievable transceiver data rates. The Xilinx GTH transceivers are designed to operate from 500 Mb/s to 16.375 Gb/s while Altera GX and GS transceivers operate from 600 Mb/s to 14.1 Gb/s, depending upon the installed FPGA speed grade. To achieve these data rates, careful board design is required, including the following techniques to reduce signal attenuation, crosstalk and impedance discontinuities:

- Use of a low-loss dielectric material
- Routing as striplines on GSG layers
- Backdrilling of vias
- Use of differential GSSG vias
- Careful skew-matching along the entire length of the differential traces
- Removal of ground layers under inline components

### 2.3 Class 5 Reference Clocks

This section describes the clocking requirements for the class 5 reference clock signals on the DNTC interface.

The DNTC daughter board receives four reference clocks from clock generators on the main board (designated Transmit REFCLKs or TREFCLKs) and generates four transceiver clock references to User FPGA transceiver bank reference clock inputs on the main board (designated Receive REFCLKs or RREFCLKs).

#### 2.3.1 Transmit Clock Outputs

These four LVDS clock references shall be sourced from low-jitter clock generators on the main board, one per daughter board slot. The supported frequency range shall be a minimum of 0.16 MHz to 710 MHz. These clocks shall be DC-coupled on the mother board. These clock signals may be buffered by the daughter board and redistributed as transmit clock lines, or used as internal daughter board clock references. Each clock shall be independently programmable from the Configuration FPGA or the User FPGA.
2.3.2 Receive Clock Inputs
Each of these clock reference input lines shall be AC-coupled on the mother board to a reference clock input for the corresponding transceiver bank of the User FPGA. Note that HCSL signaling does not have to be supported on this interface.

2.3.3 Reference Clock Electrical Requirements
Transmit reference clocks shall be generated as LVDS signals and should be received on the daughter board using LVDS-compatible buffers.

The transmit reference clock outputs shall meet the following requirements:

- Frequency tolerance of +100 ppm.
- Spread-spectrum clocking not enabled by default, but may be provided as an option.
- Phase jitter requirements of PCI Express GEN 3 (0.8 ps RMS maximum, 0Hz – Nyquist (clock frequency/2)). It is highly recommended that the generated phase jitter is as low as is reasonably possible.
- LVDS output voltage: 250mV to 450mV single-ended peak-to-peak, 500mV – 900mV (650 mV nominal) differential peak-to-peak
- LVDS common-mode output voltage: +1.125 to +1.275VDC (+1.20VDC nominal)

The receive reference clocks are AC-coupled on the main board to FPGA transceiver reference clock inputs and support CML, LVPECL and LVDS signaling. Note that HCSL is not supported by the receive reference clocks since it requires DC coupling.

Since the receive reference clocks are AC-coupled, the receiver on the FPGA will re-bias the clock signal to the input common-mode voltage. For a Xilinx UltraScale FPGA, this is four-fifths of the MGTAVCC supply voltage (or +0.80VDC) while for an Altera Stratix V FPGA, this is equal to the $V_{CCR_{GXB}}$ power supply level, +1.00VDC). The differential input impedance at the FPGA is typically 100 ohms. The input AC-coupling capacitor shall be 0.01uF. The receive reference clock inputs to the mother board shall meet the following requirements:

- Differential peak-to-peak input voltage between 250mV and 2000mV (1600mV before FPGA configuration).
- Clock frequency between 100 and 710 MHz.
- Clock duty cycle between 40% and 60%.
- Meet the reference clock characteristics specified in the standard for which the transceiver block is used on the daughter board.

2.3.4 Reference Clock Routing
Transmit reference clocks are routed as closely-coupled differential pairs on internal layers, preferably GSG layers, and each pair is length-matched to within ±10 mils. There is no length-matching requirement between the four clock pairs. These signals are DC-coupled on the main board from the clock generator chip to the DNTC connector pins.
Receive reference clocks are routed as closely-coupled differential pairs on internal layers, preferably GSG layers. These signals are AC-coupled on the main board from the DNCT connector pins to the corresponding transceiver bank reference clock input pins on the User FPGA. A 0.01μF coupling capacitor is recommended. Each pair is length-matched to within ±10 mils. There is no length-matching requirement between the four clock pairs or with the transceiver signals.

2.4 Class 6 Out-of-Band I/O Signals
The Out-of-Band (OOB) bus consists of 32 signals, which can be driven differentially or single-ended. These signals are generally used to implement low-speed control signals between the User FPGA and the daughter board. Allowed signal levels are between +1.20VDC and +3.40VDC, allowing direct connection of +3.3V signals.

2.4.1 General OOB I/O Requirements
The Vcco power supply at the DNCT interface (see section 2.7.4) is used to power the I/O bank(s) of the User FPGA on the main board used for the OOB signals. The OOB bus signals are directly connected to I/O bank signals and they may not be pulled above this supply by the daughter board. Level translators should be used on the daughter board to interface the OOB lines to parts that require single-ended logic I/O at voltages other than Vcco.

**Requirement:** No OOB signals shall be pulled more than 0.30VDC above Vcco on the mother board or daughter board.

The daughter board designer should consider buffering low-speed OOB signals to isolate them from daughter board module interfaces in order to help protect the main board FPGA from ESD events originating on the daughter board.

Except possibly for the PCI Express Hard-IP Reset connections discussed below in section 2.4.4, all OOB signals shall be connected to a single I/O bank at the mother board FPGA, or to two adjacent banks, with one bank used for the “TX” signals and the other used for the “RX” signals. Each TXxxp/TXxxn and RXxxp/RXxxn pair shall be connected to a differential pair at the FPGA. For mother boards based on Xilinx FPGAs, there is no differentiation between LVDS transmitter I/Os and LVDS receiver I/Os and pairs may be assigned anywhere in the bank. For mother boards based on Altera FPGAs, the OOB “TX” pins shall be connected to LVDS transmitter pins on the FPGA and the OOB “RX” pins shall be connected to receiver pins.

**Recommendation:** Because the “TX” and “RX” signals may be connected to different banks in the FPGA, daughter board designers should group related signals on either the TX or RX pins, rather than TX/RX pairs.

2.4.2 Signaling Standards and Termination for OOB Signals
All OOB bus signals shall tolerate a single-ended voltage of between -0.3V to Vcco + 0.3V.
The mother board shall be capable of bi-directional signaling on all OOB bus signals. It shall both accept and transmit either LVCMOS, SSTL, HSTL, or LVDS levels. $V_{CCO}$ may be between +1.20 VDC and +3.40 VDC. The daughter board design shall determine the signaling standard to use and the daughter board will therefore provide an appropriate $V_{CCO}$ voltage within the defined range.

Single-Ended signaling levels, relative to the mother board I/O pins, are defined in the following table.

### Table 3 - Single-Ended Signaling Standard Voltage Level Definition

<table>
<thead>
<tr>
<th>Signaling Std</th>
<th>$V_{IL _MIN}$</th>
<th>$V_{IL _MAX}$</th>
<th>$V_{IH _MIN}$</th>
<th>$V_{IH _MAX}$</th>
<th>$V_{OL _MAX}$</th>
<th>$V_{OH _MIN}$</th>
<th>$I_{OL}$ (mA)</th>
<th>$I_{OH}$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSTL_I</td>
<td>-0.300 $V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$V_{CCO} + 0.300$</td>
<td>0.400</td>
<td>$V_{CCO} - 0.400$</td>
<td>8.0</td>
<td>-8.0</td>
<td></td>
</tr>
<tr>
<td>HSTL_II</td>
<td>-0.300 $V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$V_{CCO} + 0.300$</td>
<td>0.400</td>
<td>$V_{CCO} - 0.400$</td>
<td>8.0</td>
<td>-8.0</td>
<td></td>
</tr>
<tr>
<td>HSTL_II_18</td>
<td>-0.300 $V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$V_{CCO} + 0.300$</td>
<td>0.400</td>
<td>$V_{CCO} - 0.400$</td>
<td>16.0</td>
<td>-16.0</td>
<td></td>
</tr>
<tr>
<td>HSTL_II_18</td>
<td>-0.300 $V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$V_{CCO} + 0.300$</td>
<td>0.400</td>
<td>$V_{CCO} - 0.400$</td>
<td>16.0</td>
<td>-16.0</td>
<td></td>
</tr>
<tr>
<td>HSUL_12</td>
<td>-0.300 $V_{REF} - 0.130$</td>
<td>$V_{REF} + 0.130$</td>
<td>$V_{CCO} + 0.300$</td>
<td>20% $V_{CCO}$</td>
<td>80% $V_{CCO}$</td>
<td>0.1</td>
<td>-0.1</td>
<td></td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>-0.300 35% $V_{CCO}$</td>
<td>65% $V_{CCO}$</td>
<td>65% $V_{CCO}$</td>
<td>0.400</td>
<td>$V_{CCO} - 0.400$</td>
<td>4/8/12 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>-0.300 35% $V_{CCO}$</td>
<td>65% $V_{CCO}$</td>
<td>65% $V_{CCO}$</td>
<td>0.450</td>
<td>$V_{CCO} - 0.450$</td>
<td>4/8/12/16 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>-0.300 35% $V_{CCO}$</td>
<td>65% $V_{CCO}$</td>
<td>65% $V_{CCO}$</td>
<td>0.450</td>
<td>$V_{CCO} - 0.450$</td>
<td>4/8/12/16 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVCMOS25</td>
<td>-0.300 0.700</td>
<td>1.700</td>
<td>$V_{CCO} + 0.300$</td>
<td>0.400</td>
<td>$V_{CCO} - 0.400$</td>
<td>4/8/12/16 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVCMOS33</td>
<td>-0.300 0.800</td>
<td>2.000</td>
<td>3.400</td>
<td>0.400</td>
<td>$V_{CCO} - 0.400$</td>
<td>4/8/12/16 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVTTL</td>
<td>-0.300 0.800</td>
<td>2.000</td>
<td>3.400</td>
<td>0.400</td>
<td>$V_{CCO} - 0.450$</td>
<td>4/8/12/16 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSTL12</td>
<td>-0.300 $V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$V_{CCO} + 0.300$</td>
<td>$V_{CCO} / 2 - 0.150$</td>
<td>$V_{CCO} / 2 + 0.150$</td>
<td>14.25</td>
<td>-14.25</td>
<td></td>
</tr>
<tr>
<td>SSTL135</td>
<td>-0.300 $V_{REF} - 0.090$</td>
<td>$V_{REF} + 0.090$</td>
<td>$V_{CCO} + 0.300$</td>
<td>$V_{CCO} / 2 - 0.150$</td>
<td>$V_{CCO} / 2 + 0.150$</td>
<td>13.0</td>
<td>-13.0</td>
<td></td>
</tr>
<tr>
<td>SSTL135_R</td>
<td>-0.300 $V_{REF} - 0.090$</td>
<td>$V_{REF} + 0.090$</td>
<td>$V_{CCO} + 0.300$</td>
<td>$V_{CCO} / 2 - 0.150$</td>
<td>$V_{CCO} / 2 + 0.150$</td>
<td>8.9</td>
<td>-8.9</td>
<td></td>
</tr>
<tr>
<td>SSTL15</td>
<td>-0.300 $V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$V_{CCO} + 0.300$</td>
<td>$V_{CCO} / 2 - 0.175$</td>
<td>$V_{CCO} / 2 + 0.175$</td>
<td>13.0</td>
<td>-13.0</td>
<td></td>
</tr>
<tr>
<td>SSTL15_R</td>
<td>-0.300 $V_{REF} - 0.100$</td>
<td>$V_{REF} + 0.100$</td>
<td>$V_{CCO} + 0.300$</td>
<td>$V_{CCO} / 2 - 0.175$</td>
<td>$V_{CCO} / 2 + 0.175$</td>
<td>8.9</td>
<td>-8.9</td>
<td></td>
</tr>
<tr>
<td>SSTL18_I</td>
<td>-0.300 $V_{REF} - 0.125$</td>
<td>$V_{REF} + 0.125$</td>
<td>$V_{CCO} + 0.300$</td>
<td>$V_{CCO} / 2 - 0.470$</td>
<td>$V_{CCO} / 2 + 0.470$</td>
<td>8.0</td>
<td>-8.0</td>
<td></td>
</tr>
<tr>
<td>SSTL18_II</td>
<td>-0.300 $V_{REF} - 0.125$</td>
<td>$V_{REF} + 0.125$</td>
<td>$V_{CCO} + 0.300$</td>
<td>$V_{CCO} / 2 - 0.600$</td>
<td>$V_{CCO} / 2 + 0.600$</td>
<td>13.4</td>
<td>-13.4</td>
<td></td>
</tr>
</tbody>
</table>

LVDS levels are defined in the following table.

### Table 4 - LVDS Voltage Level Definition

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Common-Mode Voltage</td>
<td>$+0.300V$</td>
<td>$+1.200V$</td>
<td>$+1.425V$</td>
</tr>
<tr>
<td>Input $dV_{pp}$</td>
<td>100mV</td>
<td>350mV</td>
<td>600mV</td>
</tr>
<tr>
<td>Output Common-Mode Voltage</td>
<td>$+1.000V$</td>
<td>$+1.250V$</td>
<td>$+1.425V$</td>
</tr>
<tr>
<td>Output $dV_{pp}$</td>
<td>247mV</td>
<td>350mV</td>
<td>600mV</td>
</tr>
</tbody>
</table>

---

6) Taken from Table 8 of Xilinx DS893, “Virtex UltraScale Architecture Data Sheet”, v1.0 dated July 10, 2014
7) Taken from Table 17 of Xilinx DS893, “Virtex UltraScale Architecture Data Sheet”, v1.0 dated July 10, 2014
8) $dV_{pp}$ is defined as ($(P-N)-(N-P)$) of the single-ended waveform. It is thus, by definition, the sum of the single-ended $V_{pp}$ values of the P and N signals.
The mother board shall implement selectable 100Ω differential termination on all OOB differential pin pairs. The mother board shall provide selectable 50Ω “thevenin” termination for single-ended inputs and controlled-impedance drivers for single-ended outputs. The daughter board shall terminate mother board outputs appropriately.

2.4.2.1 VREF Provision
Two VREF pins are provided on the DNCT connector to provide an external reference voltage for the FPGA I/O banks connected to the “TX” and “RX” OOB pins, respectively. For mother boards that use a single bank for both sets of OOB signals, the “TX” VREF pin shall be connected and the “RX” VREF pin shall be left floating. Daughter boards may either connect a reference voltage between ground and VCCO to a VREF pin or, if not used, connect it to ground through a 500 ohm resistor. Daughter boards shall always connect both VREF pins.

2.4.2.2 Power-On Sequencing Requirements Related to OOB Signals
No OOB bus pin shall be driven above VCCO + 0.3VDC by either mother board or daughter board. To meet this requirement it is recommended that both mother board and daughter board use VCCO as the VCC rail for their I/O buffers.

2.4.3 Signal Routing Requirements
OOB signals shall be routed as 100Ω differential pairs / 50Ω single-ended signals. Loosely coupled routing is required. It is assumed that high-speed OOB signaling will be accomplished using LVDS on these differential pairs, and that general-purpose single-ended signaling on the OOBs will be relatively low-speed and hence insensitive to cross-talk due to the coupled pairs. If a high-speed single-ended signal is required over the OOB bus, the corresponding signal within the differential pair should be defined as a static level in order to avoid potential cross-talk issues.

Recommendation: The daughter board designer should carefully consider potential cross-talk issues between the differential pairs within the OOB bus when they are used for single-ended signaling.

OOB differential pairs shall be P/N length-matched to within 10 mils on the main board, and all of the OOB signals shall be length-matched to within 500 mils on the main board. It is recommended that length-matching is done as closely as possible. Length-matching on the mother board shall account for the internal trace lengths within the FPGA device.

The daughter board has no specific signal routing requirements. Constraints for daughter board routing are application dependent and shall thus comply with any interface requirements, given the mother board routing mentioned earlier.

2.4.4 PCIe Hard-IP Reset Connections
The User FPGAs may contain PCI Express Hard-IP (HIP) blocks, which have a fixed relationship with external transceiver banks. The reset signals associated with these PCIe HIP blocks may be hard-mapped to specific FPGA pins and may not be accessible using GPIO pins via the logic array. Therefore, if HIP PCIe blocks with fixed reset pins are connected to DNCT transceiver lanes, the OOB connections
must include the reset signals, even if these signals are not in the bank(s) otherwise connected to the DNCT OOB bus. Therefore, in this case, the following connections must be made on the mother board:

**OOB14_TX7p** – Optionally, via an uninstalled zero-ohm resistor, used for the hard reset signal for a PCIe HIP block connected to transceiver bank 0. By default, this pin is connected via a zero-ohm resistor to an appropriate pin in the “TX” I/O bank.

**OOB15_TX7n** – Optionally, via an uninstalled zero-ohm resistor, used for the hard reset signal for a PCIe HIP block(s) connected to transceiver banks 1 to 3. By default, this pin is connected via a zero-ohm resistor to an appropriate pin in the “TX” I/O bank.

If an ENDPOINT mode PCIe interface is implemented on the daughter board, the associated PERSTn signal must be mapped to one of the two indicated OOB pins, depending on which transceiver bank(s) is (are) used to implement the PCIe data lanes.

Any ROOT mode PCIe interfaces on the daughter board must isolate the PCIe HIP reset input from the interface PERSTn signal to avoid resetting the HIP block. In this case, the associated OOB pin must be pulled to a high logic level.

Daughter boards that do not implement PCIe interfaces may use the OOB14_TX7p and OOB15_TX7n pins for general-purpose signaling.

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**Design note:** A daughter board implementing a PCIe interface may require mother board resistor changes as described above to make the correct reset connections.

---

### 2.4.5 Clock-Capable Connections

Two OOB differential pairs shall be connected to User FPGA global clock inputs on the mother board. This allows the daughter board to directly drive global clock trees or local PLLs within the FPGA, as required. The following OOB pairs shall be clock capable: **OOB28_CLK_RX6p/OOB29_CLK_RX6n and OOB30_CLK_RX7p/OOB31_CLK_RX7n**.

---

### 2.5 Class 7 Management Bus Signals

The DNCT management bus will generally only be used for managed daughter boards. An alternate use of the DNCT management bus signals is as a daughter board FPGA configuration interface. In this mode, they implement a serial configuration interface that can be used to program a daughter board-hosted FPGA from the mother board. The usage of the management bus interface signals depends upon the programming of the Configuration FPGA on the mother board.

When configured as a management bus, the bus is suitable for low-speed signaling only. See Section 2.5.1.2 for details on managed daughter board design. Signals CS#, A0, A1, SCK, MOSI, and MISO implement an “enhanced” 4-wire SPI-type serial bus connection between the Configuration FPGA on the mother board, and a CPLD on a managed daughter board. Signal INT# is used to convey daughter board
interrupts to the main board control processor via the Configuration FPGA. Signal MGMT_RST# allows the main board processor to reset the daughter board.

2.5.1 Managed vs. Unmanaged DNTE Daughter Board Design
Two basic categories of DNTE daughter boards are defined, specifically “managed” and “unmanaged” types. A managed daughter board makes use of the management bus, which allows the main board microprocessor to monitor and control I/O modules and/or other resources on the daughter boards through the Configuration FPGA. Unmanaged daughter boards do not implement a direct management path, relying instead on user IP running on the User FPGA for most, if not all, daughter board-related configuration and control functions. This section presents conceptual design examples for both types of daughter boards.

2.5.1.1 Unmanaged Daughter Boards
On unmanaged DNTE daughter boards, all module control lines are implemented using single-ended low-speed OOB I/O. This requires that all I/O module configuration and control functions are implemented using logic circuitry in the User FPGA.

The management bus signals are not connected on unmanaged daughter boards or are used for other functions, such as the DNTE Daughterboard Configuration Interface described in section 2.5.6.

A CPLD is generally only required on a managed daughter board. However, a CPLD might be required on an unmanaged daughter board if the number of I/O module control lines exceeds the number of available OOB signals. In this case the CPLD serial interface would be connected using OOB signals.

2.5.1.2 Managed Daughter Boards
On managed daughter boards, the management interface signals are connected to a CPLD, including the I/O board chip select (CS#), serial clock (SCK), serial data lines (MOSI, MISO), and two SPI bus address bits (A[1:0]). The CPLD implements an address decoder with signal buffering and signal steering logic, reset and interrupt logic, and a standard slave SPI peripheral. This slave peripheral is used to implement control registers and GPIO, which are used to interface with control lines on the daughter board.

Managed daughter boards should store a daughter board ID code in a reserved location within the ID/EEPROM space (see Table 5 above). Note that unmanaged daughter boards will return a daughter board ID value of 0xFFFF when queried at this address since a pull-up is used on the serial data line on main board. This will be a reserved daughter board_ID code, which will be used to identify an unmanaged daughter board. The presence detect pin at the DNTE interface can be used to differentiate an empty slot from a slot occupied by an unmanaged daughter board.

2.5.2 Management Bus Electrical Requirements
The DNTE management bus shall be connected to a +1.8V I/O bank on the Configuration FPGA on the mother board. Devices connected to these pins on the daughter board must be compatible with +1.8V.

---

9 There have been no managed daughter boards designed or constructed as of the date of this document. Note that the management bus circuitry would also need to be designed for the Configuration FPGA in order to complete a managed DNTE system.
CMOS signaling levels, as defined in the Xilinx UltraScale Virtex datasheet (DS893) or the Stratix V Device Datasheet (SV53001). The Vcc0 power supply shall be +1.80V ±5% on both the mother board and the daughter board.

Except as noted, the mother board (all signals except MISO and INT#) or daughter board (on MISO) shall use push-pull drivers on all management bus signals. The mother board shall provide 4.70K pulldown resistors to ground on all management bus signals except INT#, which shall have a 4.70K pullup to the +1.80VDC power supply.

### 2.5.3 Management Bus Routing

The DNTC management bus signals are routed as single-ended traces on standard GSSG layers. The address and data lines may be bussed to multiple DNTC daughter board slots, while the chip select, clock, interrupt, and reset lines are routed point-to-point from the Configuration FPGA to individual DNTC connectors.

### 2.5.4 Management Bus Signal Descriptions

This section describes the purpose and function of each of the Class 7 signals in the management bus mode.

#### 2.5.4.1 SPI Bus (SCK, MOSI, MISO, CS#)

The management SPI Bus connects a master in the FPGA on the mother board with a slave in a CPLD on the daughter board, using SPI mode (0, 0) with CPOL = 0 (base level of the clock is logic 0) and CPHA = 0 (data is captured on the clock's rising edge and data is propagated on the falling edge). As a minimum, all mother boards and managed daughter boards shall support SPI Bus operation at a clock rate of 10MHz. Specialized mother/daughter board designs may support higher clock frequencies. Also, all mother and daughter boards shall support MOSI as a mother board output and MISO as a mother board input. Specific designs may support Double Data Rate (DDR) modes and 2-bit wide modes, where both MOSI and MISO are used as bidirectional signals. On unmanaged daughter boards, the SPI Bus signals may be left unconnected.

#### 2.5.4.2 SPI Address (A1, A0)

The two SPI Address bits, A1 and A0, are driven by the mother board and are used to steer the daughter board management bus serial interface signals to multiple daughter board SPI busses, both internal and external to the CPLD, as shown in the following table. Both address bits shall be stable whenever CS# is low. On unmanaged daughter boards, A0 and A1 may be left unconnected.

<table>
<thead>
<tr>
<th>A1</th>
<th>A0</th>
<th>SPI Bus</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>ID/EEPROM</td>
<td>Module ID register, optional serial EEPROM</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Temp Sensor</td>
<td>A temp sensor is required on dissipative daughter boards</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Spare</td>
<td>Optional internal or external SPI bus</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>GPIO</td>
<td>Control/GPIO registers internal to CPLD</td>
</tr>
</tbody>
</table>
### 2.5.4.3 PRSNT#/INT#

Following power-on and a hardware reset (see Section 2.6.5), this pin shall function as PRSNT2#, as defined in Section 2.6.2. On a managed daughter board only, a write to a reserved location within the ID/EEPROM space (see Table 5 above) shall be used to release this functionality and the pin shall become the INT# management bus signal, as described below.

The INT# management bus signal is an interrupt input to the mother board and is driven low by the daughter board to indicate an interrupt condition. The mother board shall include an input pull-up to +1.80VDC that shall not provide current less than 100μA or in excess of 2mA when the signal they pull up is shorted to ground. The daughter board shall drive INT# with either an open-drain or 1.8V push-pull driver that shall be able to sink at least 4mA at a $V_{OL}$ of +0.30VDC. On unmanaged daughter boards, PRSNT2#/INT# shall remain in its PRSNT2# setting.

### 2.5.4.4 MGMT_RST#

The MGMT_RST# signal is a mother board output intended as an active-low reset for the daughter board management bus interface and any other appropriate circuitry. MGMT_RST# shall be driven by an open-drain or 1.8V push-pull driver that shall be able to sink at least 4mA at a $V_{OL}$ of +0.30VDC. A managed daughter board shall pull the MGMT_RST# signal high to +1.8VDC with a 4.70K resistor. On unmanaged daughter boards, MGMT_RST# may be left unconnected.

### 2.5.5 Management Bus Timing

Read and write cycles for the daughter board management interface are illustrated in Figure 3. Each bus cycle consists of command, address, and data phases. Prior to accessing the interface, the system controller sets the daughter board address bits, then transfers data using the daughter board management interface, which is similar to a SPI interface. The sample management interface cycles shown in Figure 3 consist of an 8-bit command opcode, 16-bits of address, and an 8-bit data transaction, although the exact nature of the cycle will depend on the addressed peripheral. Once the controller has identified the daughter board by reading the daughter board ID register, it will be able to configure the management bus transactions accordingly. The ID/EEPROM space on all daughter boards will use the same predefined transaction format.

---

**Table 5 - Management Interface Daughter Board SPI Bus Address Bit Decode**

<table>
<thead>
<tr>
<th>Table 5 - Management Interface Daughter Board SPI Bus Address Bit Decode</th>
</tr>
</thead>
</table>

---

Rev 1.4, 2017-11-15
2.5.6 **DNTC Daughter Board Configuration Interface**

This section describes the rules pertaining to the Class 7 management bus signals when used as FPGA configuration signals. The intent of these signals is to implement a serial configuration interface that can be used to program a daughter board-hosted FPGA from the mother board.

### 2.5.6.1 Configuration Signal Interface

The Class 7 configuration signals form a sub-interface that is to a large extent independent from the rest of the DNTC interface. The only non-Class 7 signals that have relation to Class 7 signals are PWR_ON and PWR_GD. The below diagram describes the configuration interface.
The DNTC configuration sub-interface is designed to be compatible with both Xilinx “Slave Serial” and Altera “Passive Serial” configuration modes. These modes are defined in Xilinx UG470 and the Altera Stratix-5 Handbook respectively.

All Class 7 signals are to be referenced to power supplies at +1.8V ±5%. Power supplies for the daughter board and for the mother board are intended to be separate. The daughter board power supply for the configuration signals is referred to as $V_{CCO_{CFG\_DC}}$, the mother board power supply for the configuration signals is referred to as $V_{CCO\_CFG\_MB}$.

Signal functions are described in section 2.5.6.2. Power-on interface functions and power supply sequencing is described in section 2.5.6.3.

### 2.5.6.2 Signal Descriptions

This section describes the purpose and function of each of the Class 7 signals in the FPGA configuration mode.

#### 2.5.6.2.1 PROG\_B (MGMT\_RST#)

The PROG\_B signal is intended an active-low reset for the daughter board FPGA. PROG\_B will be pulled to ground with a 4.70kΩ resistor on the main board. The daughter board will pull the PROG\_B signal high to $V_{CCO\_CFG\_DC}$ with a 470Ω resistor.

PROG\_B is driven low or tri-stated by the mother board upon power-on. Once PWR\_GD has been asserted, PROG\_B will be tri-stated by the mother board. When the mother board initiates configuration, it shall pulse PROG\_B low to clear the daughter board FPGA. PROG\_B may never be driven high by the mother board, only tri-stated.
A daughter board not implementing the DNCTC Configuration Interface may leave PROG_B floating or pull it low with a resistor.

2.5.6.2.2 INIT_B (A1)
The INIT_B signal is intended to be used as a signal, driven by the daughter board, that the daughter board is ready to accept configuration. When the INIT_B signal is high, the mother board may configure the daughter board. It shall be pulled low with a 4.70kΩ resistor minimum on the main board. The daughter board will pull the INIT_B signal high to $V_{CCO_{CFG_DC}}$ with a 470Ω resistor.

Daughter boards not implementing the DNCTC Configuration Interface are recommended to connect the INIT_B signal to ground.

2.5.6.2.3 CCLK (SCK)
The CCLK signal is the clock for the serial configuration data. The mother board shall transmit CCLK; the daughter board should use CCLK to clock in data from the DIN pin on the rising edge. The signal is driven with a 1.8V CMOS driver on the main board. It shall be pulled low with a 4.70kΩ resistor on the main board. It may be pulled low with a 4.70kΩ resistor on the daughter board.

A daughter board not implementing the DNCTC Configuration Interface may leave CCLK floating or pull it low with a resistor.

2.5.6.2.4 DIN (DI)
The DIN signal carries configuration data from the mother board to the daughter board. The mother board shall drive this signal with a 1.8V CMOS driver. It shall be pulled low with a 4.70kΩ resistor on the main board. It may be pulled low with a 4.70kΩ resistor on the daughter board.

A daughter board not implementing the DNCTC Configuration Interface may leave DIN floating or pull it low with a resistor.

2.5.6.2.5 DONE (A0)
The DONE signal is an active-high signal indicating that the daughter board FPGA has been configured successfully. It shall be pulled low with a 4.70kΩ resistor on the main board. It shall be either driven by the daughter board with a 1.8V CMOS driver, or pulled to $V_{CCO_{CFG_DC}}$ with a resistor and driven with an open-drain buffer.

A daughter board not implementing the DNCTC Configuration Interface may leave DONE floating or pull it low with a resistor.

2.5.6.3 Power Sequencing
There are specific power-on sequencing requirements pertaining to the DNCTC configuration sub-interface. Since the signals are powered by separate power supplies on the mother board and daughter board, care must be taken during power-on so as not to damage the mother board or daughter board.

On the mother board, no signals may be driven high until the daughter board has asserted PWR_GD. PROG_B must be held low while PWR_GD is off. The mother board should not assert PWR_ON until $V_{CCO_{CFG_MB}}$ is within regulation.
The daughter board shall not power $V_{CCO\_CFG\_DC}$ until PWR\_ON is asserted. The daughter board shall not assert PWR\_GD until $V_{CCO\_CFG\_DC}$ is within regulation.

The mother board shall not initiate configuration until the following conditions are met:

1. PWR\_ON has been asserted by the mother board
2. PWR\_GD has been asserted by the daughter board
3. INIT\_B is high (allowed to float by daughter board)

### 2.6 Class 3 Control Signals

There are five control signals at the DNCT interface. These are used for power sequencing and interface management. Their purpose and associated requirements are described in this section.

The Reserved pins are not currently used and are available for future use.

#### 2.6.1 Driver and Pull-Up Requirements

The signals in this section specify the use of open-drain drivers and pull-ups. The requirements for these are specified below.

All open-drain drivers shall tolerate a voltage of up to +5.5VDC on their outputs, irrespective of the state of the board power rails. They shall be able to sink at least 4mA at a $V_{OL}$ of +0.45VDC.

All input pull-ups shall be to a voltage between +1.80VDC – 5% and +3.3VDC + 5%. They shall not provide current less than 100μA or in excess of 2mA when the signal they pull up is shorted to ground.

#### 2.6.2 Daughter Board Presence Detect (PRSNT# and PRSNT2#)

Pins 1 and 5 at the DNCT connector, PRSNT# and PRSNT2#, are the daughter board presence detect signals. At power-on or a hardware reset (see Section 2.6.5) the daughter board shall ground one or both of these pins and the mother board shall have pullups and inputs to the Configuration FPGA, allowing the mother board to determine that a daughterboard is installed and properly seated, as well as the usage of the Management Bus, as shown in the following table. For a managed daughter board only, a write to a reserved location within the ID/EEPROM space (see Table 5 above) may be used to release this functionality so that the pin can become the INT# management bus signal, as described in Section 2.5.4.3.

*Table 6 – Daughter Board Presence Detect Coding*

<table>
<thead>
<tr>
<th>PRSNT#</th>
<th>PRSNT2#</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Daughter board with FPGA Configuration Interface</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Management Bus pins not used</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Daughter board with Management Bus</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>No daughter board installed</td>
</tr>
</tbody>
</table>
2.6.3 **Power On**
The PWR_ON signal, on pin 313, is an active-high signal to indicate that the daughter board may power on its power supplies, including V_{CCO}. It shall be an open-drain output of the mother board with a 1.00Kohm pullup on the mother board. Before this pin goes high, neither the mother board nor the daughter board may drive the V_{CCO} supply\(^{10}\) or any of the OOB signal pins above ground.

A daughter board that requires an external power source for operation shall hold PWR_ON low using an open-drain driver until the external power is available and usable.

A daughter board may turn on internal power supplies before PWR_ON goes high or may turn on all power when it goes high.

2.6.4 **Power Good**
The PWR_GD signal, pin 315, signals to the mother board that daughter board power supplies have stabilized. It is to be an open-drain output on the daughter board and pulled high on the mother board. It must be implemented on the daughter board. The mother board shall not drive any of the I/O signal pins to the daughter board (other than PWR_ON) until PWR_GD is high.

2.6.5 **Hardware Reset**
The HW_RST# signal, pin 317, is an active-low signal to reset the circuitry on the DNCT daughter board. It shall be an open-drain output of the mother board and requires a pullup resistor on the daughter board. It typically indicates the system reset state of the mother board.

2.6.6 **VCCO Voltage Set**
Pin 319 on the DNCT connector, VCCO_SET, controls the output voltage of the V_{CCO} bias regulator on the mother board.

Normally, with an installed DNCT daughter board, the VCCO_SET pin is left floating and the daughter board provides its own V_{CCO} power supply at a voltage above the +1.35VDC bias voltage from the mother board. This higher voltage turns off the mother board regulator and the daughter board fully controls the V_{CCO} voltage and provides all of the current required for both mother board and daughter board circuitry.

The VCCO_SET pin is used for two situations:

1) If a daughter board has its own supply voltage at +1.35VDC or lower, it can connect VCCO_SET through a resistor to the V_{CCO} power supply, reducing the bias voltage from the mother board, so that it does not interfere and try to drive the power rail.

2) Daughterboards with limited V_{CCO} power requirements that can be supplied by the bias supply on the mother board may use the VCCO_SET pin to modify the V_{CCO} supply voltage and not include their own supply.

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\(^{10}\) Some feed-through on V_{CCO} is acceptable provided it does not exceed +0.7VDC.
Raising or lowering the bias voltage is done by connecting a resistor between VCCO_SET and ground or the Vcc power supply, respectively. The resistor must be located next to the connector pin on the daughter board, with both ends routed using the shortest traces possible, to minimize noise pickup. The available voltage range from the bias supply is +1.20VDC to +3.00VDC.

The mother board must use a TPS74201 1.5A Ultra-LDO from TI as the Vcc regulator, or another regulator with the same output voltage set pin characteristics. The voltage set circuitry on the mother board shall be as shown in Figure 5. The threshold voltage at the set pin of the regulator is +0.800 ±0.004VDC at TJ = 25°C. With the indicated circuitry, the voltage characteristics of Vcc are (approximately ±2% tolerances on all voltages):

VCCO_SET open - Vcc = +1.3515VDC (0.11% over +1.35V)

VCCO_SET grounded - Vcc = +2.9715VDC (0.95% below +3.00VDC)

VCCO_SET connected to Vcc through a 9.18K resistor - Vcc = +1.224VDC = +1.200VDC + 2%

VCCO_SET grounded through a resistance R (KΩ) - Vcc = 1.3515 + 2.1712 / (R + 1.60K)

VCCO_SET connected to Vcc through a resistance R (KΩ, 9.18K minimum) - Vcc = 0.8 + 0.5515 * (R + 1.60K) / (R + 4.84K)

The absolute minimum Vcc voltage is +1.20VDC (not +1.2VDC – 5%). To insure this, the minimum allowed resistance at VCCO_SET when connected to Vcc is 9.18K.

**CAUTION:** The mother board may use other I/O signals in the DNTC banks on the FPGA that require a minimum Vcc voltage of +1.20VDC. Therefore, the daughter board must guarantee a voltage setting of no less than this, minimum, during normal operation.

**CAUTION:** If a daughter board is supplying a Vcc near or below +1.35VDC, it must use VCCO_SET as shown above to reduce the voltage of the bias regulator on the main board so that it does not interfere.

![Figure 5 – Mother Board DNTC VCCO_SET Circuitry](image-url)
2.6.7 **Reserved Interface Pins**
The reserved pins on the DNTC connector may be defined by future main boards in order to expand DNTC functionality. These pins shall not be connected on the mother board, except to fan them out to vias for debug and prototyping use. They should likewise be fanned-out on the daughter board, if possible.

2.7 **Power Provisions**
This section details the Class 1 and 2 power delivery signals on the DNTC interface.

Three power rails are available across the DNTC interface header: +12VDC and +3.3VDC for daughter board power and $V_{CCO}$ to power the Out of Band bus I/O bank. The +12VDC and +3.3VDC power rails are sourced from the mother board while the $V_{CCO}$ power rail is biased on the mother board but typically powered by the daughter board.

2.7.1 **Ground Pins**
There are many ground pins on the DNTC interface headers. These serve as both as digital ground (i.e. signal return paths and digital power supply grounds) and chassis ground. They shall be connected to digital ground on both mother and daughter boards.

2.7.2 **+12VDC Power Rail**
The +12VDC power rail shall be driven by the mother board; it shall provide a voltage of $+12V \pm 10\%$. It is intended for use as an input voltage for switching power supplies. The mother board shall provide at least 10A on this rail and a DNTC daughter board shall draw no more than 10A. This power rail shall be supplied directly from the mother board’s input power and is energized at the same time as the mother board.

The mother board shall include a 20A fuse in-line with this supply. It is recommended that a 20A or greater fuse be installed in-line on the daughter board for this rail.

2.7.3 **+3.3VDC Power Rail**
The +3.3VDC power rail shall be driven by the mother board; it shall provide a voltage of $+3.3V \pm 5\%$. It is intended for use as an input voltage for switching power supplies. The mother board shall provide at least 1.0A on this rail and a DNTC daughter board shall draw no more than 1.0A. Daughter boards with modest power requirements (< 3.3W) can use this rail exclusively for their power. However, the +3.3VDC rail may not be energized at the beginning of the mother board power-up sequence.

The mother board shall include a self-resetting PTC fuse with a 1.5A nominal hold-current rating in-line with this supply. It is recommended that a 2A or greater fuse be installed in-line on the daughter board for this rail.

2.7.4 **$V_{CCO}$ Rail**
The $V_{CCO}$ rail is intended for use as a reference voltage for the OOB bus signals (see section 2.4), and as a source power supply for the I/O buffers used for this bus.
2.7.4.1 Daughter Board Interface Requirements
The voltage on the V\textsubscript{CCO} rail when a daughter board is installed shall be between +1.224VDC and +3.30VDC, nominal (+1.200VDC to +3.465VDC, maximum). The mother board shall provide a power supply that biases the V\textsubscript{CCO} rail to +1.35VDC ±5% when a daughter board is installed. This supply shall provide a minimum of 500mA of current when the V\textsubscript{CCD} voltage is at +1.20VDC. The available current may increase at higher V\textsubscript{CCO} voltages. This supply shall shut down if a daughter board impresses a higher voltage on the V\textsubscript{CCO} rails.

The V\textsubscript{CCO} rail shall normally be driven by the daughter board and the biasing power supply on the mother board is not used to power a daughter board interface. For daughterboards whose V\textsubscript{CCO} power requirements are under 500mA total for both sides of the interface, the mother board biasing supply may be used to power both sides of the interface. In this case, the voltage of the mother board biasing supply may be modified from its nominal +1.35VDC level as explained in Section 2.6.6. If a daughter board requires a VCCO voltage less than +1.35VDC (or at +1.35VDC but at a current higher than the bias supply can provide, the voltage of the mother board biasing supply may be reduced from its nominal +1.35VDC level as explained in Section 2.6.6.

The daughter board shall normally provide at least 1A of V\textsubscript{CCO} current, increasing to 2A if HSTL or SSTL signaling is to be used.

V\textsubscript{CCO} shall not come up faster than +12VDC.

2.7.4.2 V\textsubscript{CCO} Requirements for Banks with No Connected Pins
If a daughter board does not connect any of the pins on the OOB bus, it may leave V\textsubscript{CCO} unconnected. The mother board shall bias the V\textsubscript{CCO} rail to a voltage between +1.224VDC and +3.00VDC, nominal (+1.200VDC to +3.465VDC, maximum).

2.7.4.3 Power Sequencing Relative to V\textsubscript{CCO}
No OOB bus signal shall be driven above V\textsubscript{CCO} + 0.3VDC by either mother board or daughter board. To meet this requirement it is recommended that both mother board and daughter board use V\textsubscript{CCO} as the V\textsubscript{CC} rail for their I/O buffers.

The daughter board must not drive V\textsubscript{CCO} power until the Power On (PWR\_ON) signal has been asserted. See section 2.6.3 for an explanation of this.
3 Mechanical Requirements

This section will describe the mechanical requirements for the DNCTC interface. The mechanical requirements include specifying the Samtec SEAM/SEAF connectors used in the interface, describing the allowed daughter board outlines and discussing system-level considerations.

3.1 Connector Specifications

The DNCTC interface shall use the Samtec SEARAY series of connectors.

- The mother board shall use the Samtec SEAF-40-05.0-L-08-2-A-K-TR connector.
  - Dini PID 4328
- The daughter board shall use the Samtec SEAM-40-07.0-L-08-2-A-K-TR connector.
  - Dini PID 4329

It is recommended that the mother board mount the SEAF connector on the solder side of the board. The daughter board shall always mount the SEAM connector on the solder side of the board.

![SEAM/SEAF Marketing Illustration](image)

Figure 6 - SEAM/SEAF Marketing Illustration

3.2 Daughter Board Outline Definitions

This section will detail the daughter board outlines designated for the DNCTC interface. Two outline options are provided: the full-length and half-length outlines, differing only in the length of the daughterboard and the resulting circuit space provided. All daughter boards implementing the DNCTC interface shall comply with one of these daughter board outlines. Both outlines are 98mm wide and
either 80mm (half-length) or 152.5mm (full-length) long. The half-length outline and mounting holes fit completely into those specified for full-length cards. Thus, half-length daughter boards may be used in motherboard positions designed for either half-length or full-length daughter boards. Full-length daughter boards may only be used in motherboard positions designed for full-length motherboards.

It is recommended that the motherboard provide space for the full-length daughter board outline and provide corresponding mounting holes, either on the motherboard or on the chassis. The motherboard shall have matching mounting holes wherever the motherboard overlaps a daughter board outline mounting hole.

A daughter board implementing either outline option must cover the entire outline and implement all mounting holes. The sides of the board have a restricted component height limitation on the front of the board to insure that adjacent cable connectors can be disconnected.

Exceptions to the requirement to cover the entire outline may be made when an off-board connector placed on the daughter board requires a cut-out or “notch” in a side or end of the board. In this case the daughter board outline may be resized as appropriate.

3.2.1 Half-length Daughter Board Outline

Figure 7 shows the half-length DNTC daughter board outline. It is shown from the component side of the daughter board, with the DNTC connector on the back side of the board and pin 1 located as shown.
3.2.2 Full-length Daughter Board Outline

Figure 8 shows the full-length DNTC daughter board outline.

All dimensions in mm

The DNTC connector is mounted on the solder side of the board and this view is through the PCB.

*Figure 8 - Illustration of Full-length DNTC Daughter Board Outline*
3.2.3 DNBC/DNTC Daughter Board Outlines
The half-length DNTC mounting hole pattern is identical to the mounting hole pattern for the main body of a DNBC Daughter Board\textsuperscript{11}. It is recommended that the mother board provide common mounting holes for a DNBC Daughter Board and a DNTC Daughter Board, where possible. There are two possible orientations of the two boards, LEFT and RIGHT, as shown in Figure 9. While custom boards may use either orientation, standard boards shall use the RIGHT orientation. While a half-length DNTC board is shown, the combined board may extend upwards to the full-height outline.

\textit{Figure 9 - Combined DNBC/DNTC Daughter Boards}

\textsuperscript{11} See the DNBC Interface Specification, Revision 0.2, dated 2015-01-30, or subsequent revisions.
3.2.4 Example Daughter Board Layouts
This section features some example DNTC daughter board layouts. This section does not contain any recommendations or requirements; it exists solely to illustrate how the DNTC interface daughter board outlines may be adapted for common use cases. The DNBTC_FMC-HPC is an example of a combined DNBC/DNTC daughter board, with both low-speed and high-speed interfaces to the mother board.

Figure 10 - Example Layouts for DNTC Daughter Boards
3.3 Daughter Board Mezzanine Stack Description
This section will describe the mezzanine stack for DNCTC daughter boards. Included will be a specification for the hardware used, spacing requirements and drawings for mated connector systems.

3.3.1 Mounting Hole Coverage and Attachment
All mounting holes in each outline shall be used to secure the daughter board and mother board together. If the mother board does not cover the extent of some of the daughter board outline and (necessarily) lacks the appropriate mounting holes, adequate support for the daughter board must be provided.

The daughter board must always fill the entire outline and hence shall implement all mounting holes called out in this specification. See section 3.1 for more information about daughter board outlines and mounting hole locations.

3.3.2 Stack Illustration
The DNCTC interface specification assumes that the SEAF connector is mounted on the top side of the mother board and the SEAM connector on the solder side of the daughter board. The DNCTC interface stack assumes no baseplate directly on the back side of the mother board. The stack for all DNCTC interfaces is illustrated below:

![Daughter Board Stack Diagram](image)

*Figure 11 - Illustration of Stack for all DNCTC Applications*

This section will detail the mechanical requirements of the DNCTC interface with regards to the mezzanine-style stacking orientation.

3.3.2.1 Clearance Requirements
The main board shall have top side components (between the main board and daughter board) no taller than 5.35mm where the daughter board outline overlaps the main board. The main board is recommended to have a thickness of 0.100”.

The daughter board shall have backside components (between the daughter board and the mother board) no taller than 4.00mm. The daughter board is recommended to have a thickness of 0.062”. The DNCTC interface makes no recommendations for component side component heights for daughter boards in non-chassis applications except along the sides of the board, where component heights are on the front of the board to insure that adjacent cable connectors can be disconnected.
It is recommended that the top surface of any components taller than 2mm between the two boards be either electrically insulated or shorted to digital ground.

3.3.2.2 Hardware Requirements
It is required that the mainboard is attached to the daughter board using five 4.5mm hex, 12mm" long, female-female, M3-threaded standoffs. It is recommended that these standoffs be stainless-steel.

It is required that the main board and the daughter board be attached to the standoffs using 6mm long screws, threaded with M3 threads. It is recommended that they be Phillips-head socket screws made of alloy steel with zinc plating.

Suggested stack mounting hardware:

**McMaster-Carr 94868A168** Female Threaded Hex Standoff, Metric, 18-8 Stainless Steel, 4.5mm Hex, 12mm Length, M3 Screw Size (Dini PID 4514)

**McMaster-Carr 91239A111** Button-Head Socket Cap Screw, Class 10.9 Alloy Steel, M3 Size, 6 mm Length, .5 mm Pitch (Dini PID 4513)

3.3.2.3 Mechanical Assembly Illustration
The following is a mechanical assembly illustration for the standoff and board mezzanine stack.

![Figure 12 - Board Mezzanine Stack Assembly Illustration](image)

3.4 Chassis and System-Level Requirements for DNCTC Implementations
This section will describe chassis and system requirements for boards implementing the DNCTC interface. In particular, the location of the chassis rear panel and connector placement guidelines will be described. Power dissipation requirements will also be addressed.

3.4.1 Daughter Board Component Height Limitation
In section 3.3.2.1 we defined the daughter board solder side component height limitations. The daughter board component side height limit shall be 27mm. It is recommended that any components taller than 4mm have their tops be either insulated or shorted to digital ground.
3.4.2 Daughter Board Cabling
External connections to a DNCTC daughterboard shall be made at the top edge of the board or using vertical connectors on the component side of the board. No connections shall be made along the sides of the board.

3.4.3 Power Dissipation
The system design shall make provision for the daughter board to dissipate the maximum rated power that the DNCTC interface provides via the Class 1 Power pins (section 2.3.3). Any additional power dissipation on the card, made possible (for example) through an external power header, is not accounted for by the system-level provisions of the DNCTC specification.

The chassis shall provide an ambient air temperature of no warmer than 50°C. There is no minimum chassis airflow guaranteed for the DNCTC daughter board.

3.4.4 Daughter Board Power Monitoring
Within space constraints, DNCTC daughter boards shall provide green LEDs to indicate that +12VDC and/or +3.3VDC power is available (i.e., the fuse has not blown) and one red LED for each power supply to indicate that it is not within approximately ±5% of its nominal value. Within space constraints, DNCTC daughter boards shall use a window comparator for each supply, checking for both undervoltage and overvoltage conditions.
Appendix A. Design Check Lists

This section provides check lists to help validate mother board and daughter board designs.

A.1. Mother Board Check List

☐ All pins on the DNTC connectors are connected as specified. If there have to be exceptions, a warning is included in the User’s Manual.

☐ The mother board is designed with an appropriate low-loss material and the transceiver signals are routed as recommended for high-frequency signals.

☐ All Class 4 and 5 signals are connected to the proper FPGA transceiver pins, meeting the required signaling standards.

☐ All Class 6 (OOB) signals are connected to I/O pins on the User FPGA capable of +3.3V operation. They are connected either to one or two adjacent I/O banks, as specified.

☐ The Class 3 (Control) and Class 7 (Management Bus) signals are connected either directly or through appropriate buffers to the Configuration FPGA.

☐ All transceiver signals, data and reference clocks, are routed on GSG layers using tightly-coupled routing and meeting all of the length-matching requirements. Internal FPGA lengths are included as part of the length-matching.

☐ All transceiver data signals are DC-coupled, both transmit and receive.

☐ Transmit reference clock outputs are generated by appropriate low jitter clock generators capable of operation from 0.16 to 710 MHz. Their frequencies can be set independently for each DNTC slot, and the signals are DC-coupled LVDS.

☐ Receive reference clock inputs are AC-coupled and support CML, LVPECL and LVDS input signaling.

☐ All Class 6 (OOB) interface signals are routed as loosely coupled 100 ohm differential pairs, meeting all of the length-matching requirements. Internal FPGA lengths are included as part of the length-matching.

☐ The defined OOB input clock-capable pins at the connector are connected to appropriate clock input pins on the FPGA.

☐ The Management Bus is designed to support its use as either a Management Bus or as a daughter board configuration interface.

☐ Both PRSNT# and PRSNT2# are routed to the Configuration FPGA to determine the type of daughter board installed. Both include pullups.
The PWR_ON and HW_RSTn outputs are open-drain outputs, capable of operation up to +5.5VDC.

The PWR_GD input has a pullup and is routed to the Configuration FPGA.

The +12VDC and +3.3VDC rails to each DNTC interface includes an appropriate series fuse and can provide up to 10A and 1.0A, respectively, to a daughter board.

The VCCO bias supply is turned off unless PWR_ON for the DNTC interface is high. When a daughter board is installed, the bias voltage shall be +1.35VDC.

The VCCO bias supply shuts down (or draws some minimal current) when a higher VCCO voltage is provided by a daughter board, up to +3.465VDC.

The VCCO bias supply is located close to the VCCO_SET pin and has the proper resistor network at this pin to set the VCCO bias voltage as defined. The bias supply shall be settable in the range +1.200 to +3.465VDC using the VCCO_SET pin.

Each DNTC interface position provides clearance for a DNTC daughter board (both half-length and full-length), without interference from other components or the chassis. It is properly aligned with a DNBC interface position, such that a single set of mounting holes is provided for both.

All specified mounting holes are provided at each DNTC interface.

Top side components under the DNTC daughter board outline are less than 5.35mm tall.

A.2. Daughter Board Check List

All class 1, 2 and 3 interface signals are connected and terminated properly.

Unused transceiver receive inputs are grounded. All other unconnected interface signals are left unconnected.

The transceiver connections in bank 4 do not assume that the mother board connects them all to the same FPGA transceiver bank.

Both transmitter and receiver transceiver connections assume DC-coupling on the mother board and include appropriate coupling and biasing circuitry to match both the DNTC and external transceiver interface requirements.

All transceiver and reference clock signals are routed as close-coupled pairs and use length-matching and routing techniques to insure proper operation at the required external frequencies.

If the transmit reference clock inputs are used, the mother board outputs are assumed to be DC-coupled LVDS signals and appropriate coupling and biasing circuitry is included.
The receive reference clock outputs use CML, LVPECL or LVDS signaling and assume AC-coupling on the mother board.

The Class 6 Out-of-Band signals are used appropriately, meeting the VCCO voltage range requirements (+1.20VDC to +3.3VDC) and using available signaling standards. Where required by a signaling standard, appropriate termination is provided.

All OOB interface signals are routed appropriately, based on their usage and with length-matching based on their maximum required frequencies and any external connections are buffered to protect the FPGA on the mother board.

OOB signals are grouped on either the TX or RX pins rather than by TX/RX pairs.

The two VREF pins on the DNTC connector are either terminated to ground or are both connected to an appropriate reference voltage.

Any clock inputs are preferentially connected to the defined clock-capable pins on the DNTC connectors.

If the Class 7 Management Bus is connected as a management bus, it uses 1.8V signaling and is connected to a CPLD on the daughter board to respond to the bus, including the decoding of the SPI address spaces. A daughter board ID code is stored in a reserved location within the ID/EEPROM address space.

If the Class 7 Management Bus is connected as a daughter board FPGA configuration interface, it is connected properly to an FPGA on the daughter board, with appropriate termination resistors.

The PRSNT# and PRSNT2# signals at the DNTC interface are grounded appropriately to indicate the usage of the Management Bus pins.

The daughter board draws no more than 10A from the +12VDC supply. If additional power is required, external connectors are provided.

The daughter board draws no more than 1.0A from the +3.3VDC supply. If additional power is required, external connectors are provided.

The daughter board either has its own VCCO supply (+1.224VDC minimum to +3.30VDC maximum) or draws no more than 500mA from the mother board’s bias supply.

The daughter board does not turn on VCCO until PWR_ON is high. VCCO is stable and operational within 0.5 seconds after PWR_ON goes high.

The PWR_GD output of the daughter board is implemented using an open-drain output. PWR_GD only goes high when all power supplies are stable and operational at their design voltage.
When a header is used to select the output voltage of a power supply (as for VCCO), the output voltage is within the allowed voltage range, regardless of how shunts are placed (no shunts, one shunt anywhere, two or more shunts).

The circuitry, if any, at the VCCO_SET pin is located close to the pin to minimize noise pickup and is designed to set the required VCCO voltage(s).

The daughter board meets the appropriate outline, including all mounting holes.

The required low-profile areas on the sides of the board are clear of any components taller than 2.0mm.

Back side components (except for the DNTC connector) are less than 4.00mm tall.

All daughter board cabling is at the top end of the board or uses vertical connectors. The cabling will not interfere with adjacent daughter boards or cables.

The daughter board includes green LEDs for the +12VDC and/or +3.3VDC supplies and red fault LEDs for the local power supplies, preferably using window comparators.