Errata Issues
This section provides a detailed description of each hardware issue known at the release time of this document.

PCI Express REFCLK Frequency

Information
Xilinx does not officially support operating the high-speed serial transceivers on Virtex-5 FXT devices at PCI Express Gen 2 (5.0Gb/s) speeds using a reference clock of 100Mhz. Instead, they require a clock multiplier external to the FPGA to raise the frequency from 100MHz to 250Mhz. The following products do not provide this external clock multiplier:

- DN9000K10PCIe8T with FX70T as FPGA Q
- DN9002K10PCIe8T with FX70T as FPGA Q
- DN9200K10PCIe8T with FX70T as FPGA Q
- DN7006K10PCIe8T with FX70T as FPGA Q
- DNMEG_V5T_PCIE with any FXT device

The following products do provide an external clock multiplier, however it is not enabled by default. Enabling the multiplier may require resistor changes to the board. Consult Dini Group for the rework instructions. Alternatively, we can make the changes here at our corporate campus in La Jolla, California.

- DN9200K10PCIe8T with FX70T as FPGA Q
As a result of this missing clock multiplier, these products will not be able to function at Gen2 rates. Operation at Gen1 rates (2.5Gb/s) is not affected by this errata.

**Symptoms**

When using a 100MHz REFCLK, transceivers will not sustain link when transitioning from Gen1 to Gen2 speeds. Depending on Core behavior, this may prevent all communication or limit linkage to Gen1 rates.

**Workarounds**

**Option 1** – There is an on-board Si5326 clock synthesizer on all affected boards that can be used to generate a 250MHz REFCLK for the serial IO (GTX) tiles of the Virtex 5. To use this clock instead of the PCI Express REFCLK, there are some minor resistor and capacitor modifications that need to be made to the board. Contact Dini Group for the rework instructions. Alternatively, we can make the changes here at our corporate campus in La Jolla, California. The Si5326 is not capable of tracking spread-spectrum (SSC) clock modulation. SSC is very common on motherboards. You must turn off spread spectrum clocking on the motherboard (usually a BIOS option) in order to use this work-around. The PCI Express revision 2.0 compliance test contains a REFCLK PLL bandwidth portion that will fail when using this work-around.

**Option 2** – Dini Group can provide a PCI Express riser board that contains a clock multiplier on it to convert the 100Mhz REFCLK provided by the motherboard into a 250MHz clock. Using this extender, the recommended 250Mhz REFCLK settings for the GTX can be used. For customers who have an affected board with FX70T devices, the riser board will be provided at no cost.

**REFCLK Jitter tolerance**

**Information**

The transceivers in the FXT family of Virtex 5 FPGAs are very sensitive to jitter on the REFCLK input of the GTX serial tiles. According to Xilinx and our own testing, PCI Express will perform reliably as long as the REFCLK signal provided by the motherboard meets the requirements of the PCI Express specification. However, we have also found that motherboards that fail to meet these specifications are quite common. The following products are affected by this issue:

- **DN9000K10PCIE8T** with FX70T as FPGA Q
- **DN9002K10PCIE8T** with FX70T as FPGA Q
- **DN7006K10PCIE8T** with FX70T as FPGA Q
- **DNMEG_V5T_PCIE** with any FXT device
LXT devices have not been reported to show this problem.

**Symptoms**

Using either the Dini Group PCIe Core and Interface or the PIPE interface with a third-party PCIe Core, the Core will periodically re-enter link training, causing the link to be unavailable for data transfer, but will eventually recover. During high PCI Express bus utilization, many retraining sequences can lead to data loss and system instability.

**Workarounds**

Option 1 – Dini Group can provide a PCI Express riser board that contains a clock jitter attenuator. Regardless of the quality of the REFCLK provided by the motherboard, this riser board will ensure that the REFCLK provided to the FXT is of very low noise.

Option 2 – There is an on-board Si5326 clock synthesizer on all affected boards that can be used to generate a low-noise REFCLK for the serial IO of the Virtex 5 FXT device. To use this clock instead of the PCI Express REFCLK, there are some minor resistor and capacitor modifications that need to be made to the board. Contact Dini Group for these rework instructions. Alternatively, we can make the change for you here at our corporate campus in La Jolla, California. The Si5326 is not capable of tracking spread-spectrum (SSC) clock modulation, which is very common on motherboards. You must turn off spread spectrum clocking on the motherboard (usually a BIOS option) in order to use this work-around. The PCI Express revision 2.0 compliance test contains a REFCLK PLL bandwidth test that will fail when using this work-around. For customers who have an affected board with FX70T devices, the riser board will be provided at no cost.

Option 3 – Use a known-good motherboard with high-quality REFCLK source. This work-around can be difficult because motherboard vendors do not typically provide the REFCLK phase noise figures for their products. Dini Group has the facilities for testing the phase noise of motherboards. The failing motherboards that we have use an NVIDIA chipset with the REFCLK signal coming directly from the north bridge chip.

**Gen2 PCI Express Spread Spectrum Clocking (SSC)**

**Information**

Most motherboards use Spread Spectrum modulation on the REFCLK signal provided to the PCI Express slots. As a result, PCI Express revision 2.0 hardware is required to track this clock modulation. The clock jitter attenuator devices on **DN9200K10PCIe8T** boards shipped before October, 2009 did not meet the PCI Express revision 2.0 standards.

**Symptoms**

Boards with the PCI Express revision 1.0 jitter attenuator will fail the PCI Express revision 2.0 compliance test, during the PLL bandwidth portion. It is unknown if this deficiency will result in communication failures.
Workarounds

Option 1 – Many motherboards implementing spread spectrum clocking have an option in the BIOS menus to disable it. BIOS menus are varied, the option to disable SSC is usually found under the ‘Advanced’ or 'chipset' sections.

Option 2 – Dini Group can replace the jitter attenuator on your board with a clock generator with a greater SSC tracking ability.

Additional Questions

Please direct any questions about this document (or other any other topic concerning Dini Group products) to support@dinigroup.com.

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