PCIe over IPASS Cable on FPGA Boards: Making it Work

We have observed a number of challenges regarding running PCIe over a 1-meter IPASS cable using the DNPCIE_CBL passive and active solutions. This document will point out the challenges and how they can be overcome.

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CHECKING THE LINK

1. Host PC is running Linux

Use the “lspci” command to see if the FPGA board was enumerated. Our reference designs will show up as a “Memory Controller” device with vendor ID “17DF”. Use “lspci –vv –d 17df:” to get detailed information about the device. The “LnkSta:” entry under the “Capabilities” section will tell you the width and speed of the link. 5GT/s corresponds to Gen2 PCIe speed. Note you will likely need root access to read the Capabilities section, if it says “access denied” in lspci then you probably don’t have root access.

Once the link has been confirmed, our AeTest Linux device driver can be compiled and installed on the system. This will work out-of-the-box for our reference designs or for connecting to the PCIEDIRECT(configFPGA) port. For a custom endpoint design the driver source code would need to be modified to identify the vendor and device ID of the endpoint.

Download the AeTest code here: http://www.dinigroup.com/files/web packs/Aetest.zip

Follow the instructions in the linuxdrv-2.6/README.txt file. The “install.sh” script can be used to build and install the driver on the system so that the driver loads automatically every time the system boots. Alternatively you can use “dndev_load.sh” to load the driver for this boot only. After the driver is loaded use “lsmod” to check that the module is present, which will be listed as “dndev”.

With the driver loaded, the AeTest program can be run. Again, this will work out-of-the-box for our reference designs. For custom endpoint designs some source code modifications will need to be made. Type “make” in the “aetest” folder to build the application, then run “aetest_linux”.

2. Host PC is running Windows

Use the “Device Manager” from Windows to see if the FPGA board was enumerated. Our reference designs will typically appear in an “Asic Emulators” category and will have vendor ID “17DF”. To get detailed information about the device, download the “SIV” tool from the internet and run it. This freely available tool will give you a wealth of information about your system including about the devices detected on the PCIe bus.

Once the link has been confirmed, our AeTest Windows device driver can be installed on the system. Windows should prompt you to install the device driver, but if it doesn’t you can go to “Device Manager”, right click on the device and select “update device driver”. Point it to the folder “AETest/wdmdrv/drv”. This driver will work out-of-the-box for our reference designs or for connecting to the PCIEDIRECT(configFPGA) port. For a custom endpoint design the driver source code would need to be modified to identify the vendor and device ID of the endpoint.

With the driver loaded, the AeTest program can be run. Again, this will work out-of-the-box for our reference designs. For custom endpoint designs some source code modifications will need to be made and the binary rebuilt. The pre-built binary is found in “AETest/aetest/aetest_wdm.exe”.

MOTHERBOARD AND CABLE ADAPTER ISSUES

1. IPASS Cable Length
All testing was done with a 1 meter IPASS x4 cable which is what we ship with all of our PCIe IPASS related products. A shorter IPASS cable may produce better results in situations where all of the below guidelines have been followed and a particular motherboard slot is still not working, but that is beyond the scope of this document. Using an IPASS cable longer than 1 meter is not recommended.

2. Active vs. Passive DNPCIE_CBL “FINGERS” Adapter Card
In the past we have supplied both active DNPCIE_CBL adapter cards, with PCIe redriver chips installed, as well as passive DNPCIE_CBL adapter cards. Moving forwards we will only be shipping the DNPCIE_CBL_PSV passive card.

The redriver chip on the active card is designed to shut down if the amplitude of the input signal drops below the specified levels. It has been found that many CPU/Motherboard combinations do not use a high enough drive strength to meet the amplitude specs at the receiver and therefore the active redriver chips simply don’t work. In all of our testing we have never seen an active DNPCIE_CBL adapter card work where the passive version did not work. For this reason we are discontinuing the active card.

<table>
<thead>
<tr>
<th>DNPCIE_CBL_PSV FINGERS Card</th>
<th>DNPCIE_CBL_ACTIVE FINGER Card (DISCONTINUED)</th>
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Figure 1: x4 IPASS Cable
3. Check LED Status and Jumper Settings on DNPCIE_CBL Adapter Card

Both the PASSIVE and ACTIVE DNPCIE_CBL Adapter cards have a “CPRSNT” LED and a “CABLE_PERSTn” LED. In normal operation the “CPRSNT” (GREEN) LED should be ON indicating that the PCIe endpoint is present, and the “CABLE_PERSTn” (RED) should be OFF indicating that PCIe Reset is not asserted.

Both the PASSIVE and ACTIVE DNPCIE_CBL Adapter cards have a “PRSNTn SEL” jumper selection with options for “1”, “4”, and “8”. In most cases setting this to “8” will allow the motherboard to detect x1, x4, and x8 endpoints. But some motherboards will fail to detect the card if you are implementing a x1 or x4 link and have the jumper set higher. Try setting the jumper to match the width of your endpoint if you are having any trouble detecting the endpoint.

On the DNPCIE_CBL_ACTIVE adapter card there is a second set of LEDs that can help diagnose problems.

“+12V” (GREEN): Indicates +12V from motherboard. Always on in normal operation.
“+3.3V” (GREEN): Indicates +3.3V from motherboard. Always on in normal operation.
“100MHz” (GREEN): Indicates 100Mhz PCIe clock from motherboard. Always on in normal operation.
“SIG_B1” (GREEN): Signal OK from motherboard on PCIe1.
   If off then motherboard drive strength is too weak.
“SIG_A1” (GREEN): Signal OK from endpoint on PCIe1.
   If off then FPGA board drive strength is too weak, or endpoint is not up.
“SIG_B2” (GREEN): Signal OK from motherboard on PCIe2.
   If off then motherboard drive strength is too weak.
“SIG_A2” (GREEN): Signal OK from endpoint on PCIe2.
   If off then FPGA board drive strength is too weak, or endpoint is not up.

NOTE: Always use IPASS cable “PCIe1”, the one nearest to the PCIe fingers for a x1 or x4 endpoint. Only use the “PCIe2” IPASS cable connection in conjunction with the “PCIe1” connection to make a x8 endpoint link.

4. Choosing A Slot On The Motherboard

Even on a single motherboard, different slots behave differently. Most notably the x16 Graphics Slots that are present on many motherboards display low drive strength characteristics. These slots are often, but not always, colored blue to designate them as the preferred graphics card slots. In many cases the drive strength on these slots is low enough that using the DNPCIE_CBL_PSV passive adapter does not work, as the signal is too weak by the time it reaches the FPGA receive pins. As stated above, the DNPCIE_CBL_ACTIVE active adapter also fails in these slots because the redriver chips shut down due to the low drive strength. Therefore these slots simply can’t be used over an IPASS cable. If enumeration fails on one slot on a motherboard it is highly recommended to try all of the slots on the motherboard before giving up entirely on that motherboard.

Figure 2: Intel BLKDZ77FA70K Motherboard
5. Boot Order
The FPGA board must be fully booted and the PCIe endpoint design must be active BEFORE the host PC is booted. The host PC will scan the PCIe bus within 1 second of power on and will not scan the bus again ever. PCIe is not a “hot-pluggable” bus and you may not add or remove PCIe devices after the host has scanned the bus. If the PCIe endpoint design is not present and fully active when the host scans the bus then it will not ever be detected until the host is rebooted or power cycled. If the PCIe endpoint is in a user FPGA on the board, and you are using the host PC to configure the FPGA, then you must reboot the PC after the endpoint design is loaded into the board so that the PC will enumerate the endpoint.

6. Performance/Bandwidth
Running PCIe over an IPASS cable will not affect the performance versus having the endpoint card plugged directly into a motherboard slot. In either case, you can expect to get roughly 650 MB/s using DMA transfer over a Gen2 x4 PCIe link between an FPGA and a host PC. For a detailed discussion see this comprehensive Xilinx white paper:

7. Motherboards We Have Tested With
Below is a list of motherboards that we have tested with and observed that PCIe Gen2 works over the 1 meter IPASS x4 cable on at least one of its PCIe slots.

Intel DX58SO2 (CPU: Intel Core i7 950 @ 3.07 Ghz)

Intel DH67BL (CPU: Intel Core i5 Quad 2400 @ 3.10 GHz)

Asus M4A79T Deluxe (CPU: AMD Athlon II X4 630 @ 2.8Ghz)
http://www.asus.com/Motherboards/M4A79T_Deluxe/

Asus P6T Deluxe V2 (CPU: Intel Core i7 920 @ 2.67 Ghz)
http://www.asus.com/Motherboards/P6T_Deluxe_V2/

Intel DP55KG (CPU: Intel Core i7 S 860 @ 2.53Ghz)

Intel DZ77GA-70K (CPU: Intel Core i5-3570K @ 3.40 Ghz)
FPGA BOARD ISSUES

1. FPGA Drive Strength
When doing PCIe over an IPASS cable the drive strength used when generating the FPGA design should be set to the maximum value (TXDIFFCTRL = 4'b1111). It was observed that using the default drive strength value in the Xilinx PCIe core resulted in some slots being unable to enumerate the endpoint, when the same slots were fully operational when the design was built with the drive strength set to the maximum.

\[
\text{TXDIFFCTRL} \quad (4'b1111)
\]

2. PCIe Clock Is 250Mhz At FPGA Pins
The PCIe clock is 100Mhz when driven over the IPASS cable by the host PC. Our FPGA boards use a jitter attenuator that also multiplies the clock up to 250Mhz before it reaches the FPGA pins. Xilinx recommends this high frequency reference clock. Make sure your PCIe design is expecting the 250Mhz reference clock frequency.

3. Check Sideband Signals For Root Complex and Endpoint Modes
Most customers connect a Host PC to a PCIe endpoint in a user FPGA, or to the PCIEDIRECT or onboard Marvell CPU endpoints. In all of these cases the FPGA board is the endpoint and the host PC is the root complex. In this configuration, the PCIe clock and reset are driven from the Host PC to the FPGA board, and the present signal is driven from the FPGA board to the Host PC. All of our boards are configured by default for endpoint mode, but the configuration should still be checked. Look in the hardware manual for the board and at the related page in the board schematic to be sure the correct components are installed and that any dipswitch settings are correct. In most cases there are socketed opto-isolator chips that should be installed by the factory. **Note that these are usual inverting opt-isolators and will invert the polarity of the sideband signals. This may make them the opposite polarity from what you expect in the FPGA design.**

Some customers put a Root Complex into a user FPGA and expect to connect a PCIe device to it through an IPASS cable interface. In this case the PCIe clock and reset must be driven by the FPGA board and present must be received from the endpoint. Some boards require only dipswitch changes to switch modes while other boards require component changes. See the hardware manual for the board in question for more details.

Note that “DOWNSTREAM” mode is the same thing as saying “The FPGA board is an Endpoint”, while “UPSTREAM” mode is the same thing as saying “The FPGA board is a Root Complex”.