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1 Overview

This document describes the DINAR1 system expansion interface. Mechanically, this interface is comprised of a single mother board and one or more expansion daughter boards, mounted in a mezzanine fashion. Provisions are made to allow the interface to work with or without a chassis. Electrically, the interface is comprised of a number of digital signals, including several clocks, and power distribution.

The goal of the DINAR1 interface is to specify a flexible and modular expansion interface that can be used to augment the functionality of off-the-shelf Dini Group ASIC Emulation systems. The principal use model is to customize features and interfaces available on a Dini Group ASIC emulation mother board, which itself hosts a FPGA, with additional memories, off-board interfaces, ADC, and DACs. Thus, the ASIC emulation system can be tailored to support an end-user’s desired feature mix.

The DINAR1 interface allows for two physical outline options, the Full-Length outline and the Half-Length outline. Compatibility between the two is driven by the mother board and system design. A Full-Length system position can host either Full or Half-Length daughter boards. A Half-Length system position can only host Half-Length daughter boards. There are no electrical differences between the Full-Length and Half-Length outline options. The only difference is the physical size of the daughter board and the space allowance made by the mother board. Section 3.1 describes the physical outline options.

The DINAR1 interface is used on several Dini Group boards including many Dini Group Xilinx 7-series ASIC emulation products. It is not backwards compatible with the Dini Group MEG Array expansion interface such as that found on the Dini Group Virtex-6 and older ASIC emulators.

1.1 Other Files

This specification makes reference to several files and drawings. They are enumerated here

1. mechanical_drawings.pdf – an annotated set of drawings describing the DINAR1 daughtercard form factor.

1.2 Terminology & Style

A variety of terminology is used throughout this document. Some of it has very specific meaning.

The phrases are to/shall/required/must state hard requirements for all cards implementing the DINAR1 interface. The words highly recommended denote characteristics that are not hard requirements, but should be implemented where possible and are likely to become requirements in future major revisions of the DINAR1 specification. The word recommended denotes characteristics that are not hard requirements nor likely to become such, but should be implemented where reasonable.

The terms “mother board,” “main board,” and “host” are used interchangeably, and refer to the FPGA-based Dini Group ASIC emulation board. The term “daughter board” or “parasite” refers to the smaller mezzanine-mounted expansion board.
1.3 Revision History

0.1 – 2012-04-03, I. Yulaev
1. Initial Revision

0.2 – 2012-04-16, I. Yulaev
1. Changed order of P/N pins in the schematic symbol (Figure 3), added V_{CCO} pins
2. Added section describing SEAC cabling (3.3.6)
3. Defined board-to-board spacing for systems (3.3.4)
4. Modified aperture plate to remove bends and revised daughterboard to chassis spacing accordingly (sections 3.3.2, 3.3.1). Also increased chassis aperture size by a few mm to ease assembly.
5. Replaced term “bulkhead” with aperture
6. Renamed spec to “DINAR1”
7. Added note in section 2.5.3 recommending tying together V_{CCO,0} and V_{CCO,1}
8. Added double-width outline spec (3.3.5)
9. Simplified mother board side length-matching requirements (2.2.2)
10. Specified that +3.3V must come up with or before V_{CCO} (2.5.3)
11. Clarified intention of daughter board pullup on PRSTN# (2.5.5.2)
12. Revised rules for V_{CCO} connection when an entire I/O bank is unused (2.5.3.2)
13. Minor edits throughout

0.3 – 2012-04-26, I. Yulaev
1. Modified Figure 2 for easier readability.
2. Specified that V_{CCO} bias supplies are ±5% (2.5.3)
3. Miscellaneous typos and minor fixes.
4. Added class 5 configuration signals and DINAR1 Configuration Sub-Interface (2.6). Updated pin description and pin map in section 2.1 and 2.4 to reflect this.
5. Revised +3.3V current limit to 2A (2.5.2)

1.0 – 2012-04-27, I. Yulaev
1. Spec ratified, promoted to revision 1.0.

1.1 – 2012-05-08, I. Yulaev
1. Added internal PID for mother board connector to section 3.2.1
2. Added section 2.1.2.1 detailing depopulation rules for partially-connected daughter board side DINAR1 interfaces.

1.2 – 2012-05-17, I. Yulaev
1. Added Samtec cable p/n to section 3.3.6

1.2 – 2012-06-22 I. Yulaev
2. Specified that the right edge of boards does not literally touch the faceplate, just faces it (section 3.1)
3. Added notes about exception in daughter card outline requirement, allowing for notches in the connector-facing edge when high-speed off board connectors require them (3.1)

1.4 – 2012-08-19 I. Yulaev
Added VRP/VRN pins to connector (class 3d) and made necessary changes to the rest of the document. Changed connector used to the 40 row, 10 column version. Removed latch posts.

1.5 – 2012-10-19 I. Yulaev
Modified Figure 41 very slightly to reflect size in chassis.
Corrected Figure 40

1.6 – 2012-10-29 I. Yulaev
Revised +3.3V current limit to 2A (2.5.2)

1.7 – 2012-11-02 I. Yulaev
Added pin A1 marker and location into all outline drawings

1.8 – 2012-11-27 I. Yulaev
Added section 2.2.1.4

1.9 – 2013-08-22 N. Harder
Fixed reference to SEAF part number in section 2.1 that called out the wrong part number.

1.10 – 2013-10-03 N. Harder
Changes to section 2.2.1.4, “Differential Termination on SCK pins”. Mother boards are now required to provide an on-board termination resistor for B1S12P/B1S12N, and shall not provide any other on-board termination resistors on any other SCK clock pins.

1.11 – 2013-10-28 N. Harder
Added Dini PID for daughter board connector to section 3.2.1.

1.12 – 2014-01-23 B. Hurley
Updated “Figure 1 - DINAR1 Interface Header Pinout” in section 2.1 to have all pin numbers ending with ‘p’ to represent the true component of a differential signal rather than ‘a’ in order be consistent with other references.

1.4 Contact
For questions or comments regarding the interface specification, contact support@dinigroup.com.
2 Electrical Requirements

This section will define electrical requirements for the DINAR1 interface. Enumerated will be requirements for signals, including signaling standards and routing requirements, as well as description of the logical interface requirements such as synchronous I/O timing information. Also in this section non-signal electrical requirements, i.e. power distribution, will be described.

2.1 Signal and Pinout Description

A pinout of the DINAR1 interface header is given below. Pin numbers follow the SEAM/SEA F pin numbering convention. All pin numbers ending with ‘p’ represent the true component of a differential signal. All pin numbers ending with ‘n’ represent the complementary component of a differential signal. The DINAR1 interface is broken up into three signal banks, plus an auxiliary set of pins consisting of control signals and power pins. Each signal bank has its own $V_{CCO}$ voltage. The control pins are referenced to the +SEQ supply.

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The below figure shows the schematic symbol for the DINAR1 mother board header (nominally Samtec SEAF-40-05.0-S-10-2-A-K-TR, see section 3.2.1). The daughter board header symbol is identical. Some annotation within the symbol is provided; this annotation will be clarified later in this document.
Figure 3 - DINAR1 Mother Board Header Schematic Symbol (ground pins omitted)
2.1.1 Signal Class Definition
This section will group the signals into signal classes, describe functionality and characteristics of the classes, and define terminology associated with them. Signals may belong to several classes at once. Note that sections 2.1 through 2.3 make minimal mention of class 1 and 2, “power” and “control” pins. These are specified in section 2.5. Class 5 “configuration” pins are described in section 2.1.1.1

Class 1 – Power
The Power pins include \( V_{CCO} \), +3.3V, and +12V.

Class 2 – Control
The Control pins are responsible for power sequencing and card detection. The control pins are PWR_GD (pin 6), +SEQ (pin 8), PRSNT# (pin 13), and PWR_ON (pin 15).

Class 3 – GPIO Signals
These are general purpose I/O pins that can be used to implement a variety of interfaces. Signal pins can be used as both single-ended (LVCMOS, SSTL, or HSTL) pins or as differential (LVDS) pin pairs.

Class 3a – Byte Groups
Byte groups are groups of 12 pins each that form a single “byte lane”. Their most common use is for high-speed memory interfaces, such as DDR DRAM or QDR SRAM. Each byte lane consists of a differential strobe pair (DQS/DQSn) and ten data/data mask/parity signals.

For a pin map that denotes the byte groups, as well as further discussion on employing a memory interface over the DINAR1, see section 2.4.

All class 3a pins are also class 3 pins.

Class 3b – Clocks
Clocks can be used to clock an interface or an entire system containing the DINAR1 interface. There are two types of clocks on the DINAR1 interface, system and local clocks. System clocks can be used to clock the entire interface\(^1\), local clocks can only be used to clock signals within the same bank.\(^2\)

All system clocks are to propagate in the downward direction, that is, from daughter board to mother board. Local clocks have directionality defined but some are downwards and some are upwards (to daughter board).

All signals in class 3b are also class 3 pins.

Class 3c – \( V_{REF} \)
\( V_{REF} \) pins can be used by the main board as a voltage reference for standards requiring it, such as SSTL and HSTL. It is to be provided by the daughter board, if the daughter board is implementing an interface that takes advantage of \( V_{REF} \).

All signals in class 3c are also class 3 pins.

---

\(^1\) Typical implementation of system clocks is to use the FPGA MRCC pins for Xilinx 7-series parts
\(^2\) Typical implementation of local clocks is to use FPGA SRCC pins for Xilinx 7-series parts
2.1.1.3.4 Class 3d – VRP/VRN
These pins are used for impedance calibration on I/O pins. They can also function as single-ended GPIO pins. These are pins S25/S0 for each bank, respectively.

All signals in class 3d are also class 3 pins.

2.1.1.4 Class 4 - Ground
All ground pins are class 4 pins. These are digital ground.

2.1.1.5 Class 5 – Configuration
Configuration signals are used to implement a serial configuration interfaces that allows the mother board to configure an FPGA hosted on the daughter board. These signals are defined as LVCMOS18 signals. They are not referenced to any of the V_{CCO} pins on the daughter board nor to any other signals on the daughter board (except GND). These signals and the rules governing their function are described in section 2.6.

2.1.2 Signal Connection Requirements
The mother board shall have all of the signals connected up appropriately. Byte groups on the daughter board interface shall be connected to corresponding byte groups on the mother board hosted FPGA. Clocks shall be connected to clock inputs on the mother board FPGA. V_{REF} pins will be connected to FPGA V_{REF} inputs.

The daughter board is not required to connect all class 3 signals; unconnected signals shall be left floating. However, all class 1 and 2 signals must be implemented in accordance with section 2.5. Class 5 “Configuration” signals should be implemented in accordance with section 2.6.

2.1.2.1 Depopulation Order
Note: The mother board is required to connect all signals on the DINAR1 interface. The rules in this section apply only to the daughter board side connections.

If a daughter board designer chooses to only partially connect the daughter board side DINAR1 connector, it is highly recommended that a particular depopulation order be followed. The signals should be depopulated in the following order:

1. Byte group 0 should be depopulated in banks 2, 1, 0, in that order.
2. Byte group 3 should be depopulated in banks 2, 1, 0, in that order.
3. Remaining signals should be depopulated in banks 2, 1, 0, in that order.

In general, entire byte groups should be depopulated one at a time, before depopulating the next byte group.

If the daughter board implements a signaling standard requiring the use of V_{REF}, both V_{REF} pins on each bank should be connected to an appropriate source, even if the rest of the byte group containing the V_{REF} pin has been depopulated.
2.2 Signaling Standards, Level Tolerance, and Routing Requirements for Class 3 Signals

This section defines the signaling standards to be employed, signaling levels to be tolerated, and physical routing requirements for class 3 (non-configuration/power) signals. In general, the approach for the mother board side of the interface is to be as flexible as possible, making provisions for both single-ended and differential signaling, minimizing skew between pairs and maximizing interface access to clock resources. The daughter board design is typically more constrained as the daughter board is geared towards implementing a specific interface.

2.2.1 Signaling Standards and Termination for Class 3 Signals

This section defines the signaling standards applicable to class 3 signals.

The below schematic clipping shows the location of these signals on the DINAR1 mother board interface header schematic symbol:
Figure 4 - Schematic Clipping Demonstrating Class 3 Signals on Mother Board DINAR1 Interface Header
All class 3 signals shall tolerate a single-ended voltage of between -0.3V to V\textsubscript{CCO} + 0.3V.

The mother board shall be capable of bi-directional signaling on all class 3 signals. It shall both accept and transmit either LVCMOS, SSTL, HSTL, or LVDS levels. V\textsubscript{CCO} may be between +1.2V – 5% and +1.8V + 5%. The daughter board design shall determine the signaling standard to use and the daughter board will therefore provide an appropriate V\textsubscript{CCO} voltage within the range defined prior.

Single-Ended signaling levels, relative to the mother board I/O pins, are defined in the following table.

Table 1 - Single-Ended Signaling Standard Voltage Level Definition

<table>
<thead>
<tr>
<th>Signaling Standard</th>
<th>V\textsubscript{IL_MIN}</th>
<th>V\textsubscript{IL_MAX}</th>
<th>V\textsubscript{IH_MIN}</th>
<th>V\textsubscript{IH_MAX}</th>
<th>V\textsubscript{OL_MIN}</th>
<th>V\textsubscript{OL_MAX}</th>
<th>V\textsubscript{OH_MIN}</th>
<th>V\textsubscript{OH_MAX}</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSTL15</td>
<td>-0.3V</td>
<td>V\textsubscript{REF} – 0.1V</td>
<td>V\textsubscript{REF} + 0.1V</td>
<td>+1.8V</td>
<td>0V</td>
<td>V\textsubscript{TT} − 0.175V</td>
<td>V\textsubscript{TT} + 0.175V</td>
<td>V\textsubscript{CCO}</td>
</tr>
<tr>
<td>SSTL18</td>
<td>-0.3V</td>
<td>V\textsubscript{REF} – 0.125V</td>
<td>V\textsubscript{REF} + 0.125V</td>
<td>+2.1V</td>
<td>0V</td>
<td>V\textsubscript{TT} − 0.470V</td>
<td>V\textsubscript{TT} + 0.470V</td>
<td>V\textsubscript{CCO}</td>
</tr>
<tr>
<td>HSTL\textsubscript{-I}</td>
<td>-0.3V</td>
<td>V\textsubscript{REF} – 0.1V</td>
<td>V\textsubscript{REF} + 0.1V</td>
<td>+1.8V</td>
<td>0V</td>
<td>0.4V</td>
<td>V\textsubscript{CCO} − 0.4V</td>
<td>V\textsubscript{CCO}</td>
</tr>
<tr>
<td>HSTL\textsubscript{-I_18}</td>
<td>-0.3V</td>
<td>V\textsubscript{REF} – 0.1V</td>
<td>V\textsubscript{REF} + 0.1V</td>
<td>+2.1V</td>
<td>0V</td>
<td>0.4V</td>
<td>V\textsubscript{CCO} − 0.4V</td>
<td>V\textsubscript{CCO}</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>-0.3V</td>
<td>+0.42V</td>
<td>+0.78V</td>
<td>+1.5V</td>
<td>0V</td>
<td>+0.4V</td>
<td>+0.8V</td>
<td>V\textsubscript{CCO}</td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>-0.3V</td>
<td>+0.45V</td>
<td>+1.05V</td>
<td>+1.8V</td>
<td>0V</td>
<td>+0.375V</td>
<td>+1.125V</td>
<td>V\textsubscript{CCO}</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>-0.3V</td>
<td>+0.63V</td>
<td>+1.17V</td>
<td>+2.1V</td>
<td>0V</td>
<td>+0.45V</td>
<td>+1.35V</td>
<td>V\textsubscript{CCO}</td>
</tr>
</tbody>
</table>

LVDS levels are defined in the following table.

Table 2 - LVDS Voltage Level Definition

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Common-Mode</td>
<td>+0.3V</td>
<td>+1.2V</td>
<td>+1.425V</td>
</tr>
<tr>
<td>Input dV\textsubscript{PP}\textsuperscript{5}</td>
<td>100mV</td>
<td>350mV</td>
<td>600mV</td>
</tr>
<tr>
<td>Output Common-Mode</td>
<td>+1.0V</td>
<td>+1.25V</td>
<td>+1.425V</td>
</tr>
<tr>
<td>Output dV\textsubscript{PP}</td>
<td>245mV</td>
<td>350mV</td>
<td>600mV</td>
</tr>
</tbody>
</table>

The mother board shall implement selectable 100\Omega differential termination on all class 3 differential pin pairs. The mother board shall provide selectable 50\Omega “thevenin” termination for single-ended inputs and controlled-impedance drivers for single-ended outputs. The daughter board shall terminate mother board outputs.

\textsuperscript{3} Taken from Table 7 of Xilinx DS183, “Virtex-7 Data Sheet”, v1.3 dated February 13, 2012
\textsuperscript{4} Taken from Table 11 of Xilinx DS183, “Virtex-7 Data Sheet”, v1.3 dated February 13, 2012
\textsuperscript{5} dV\textsubscript{PP} is defined as ( (P-N)–(N-P) ) of the single-ended waveform. It is thus, by definition, the sum of the single-ended V\textsubscript{PP} values of the P and N signals.
2.2.1.1 \( V_{REF} \) Provision
It is highly recommended that the daughter provide an appropriate \( V_{REF} \) when SSTL or HSTL signaling levels are selected. The mother board shall not be damaged by supplying a \( V_{REF} \) voltage on any of the class 3c pins. It is recommended that the mother board be capable of using a voltage supplies on any of the class 3b pins as a \( V_{REF} \) input. If the daughter board provides a reference voltage on the \( V_{REF} \) pins in any bank, all of the \( V_{REF} \) pins must be shorted electrically and used for the same purpose.

2.2.1.2 Power-On Sequencing Requirements Related to Class 3 Signals
See section 2.5.3.1.

2.2.1.3 Impedance Control and VRP/VRN Pins
The VRP/VRN pins may be used for impedance control and calibration for motherboard I/O. If this feature is used, the resistors should be sized to 2R, where R is the desired termination impedance. The VRN pin should be connected to the \( V_{CC} \) of the relevant bank and the VRP pin should be connected to ground, both through the calibration resistors.

2.2.1.4 Differential Termination on SCK pins
The mother board shall provide on-board 100\( \Omega \) differential termination on the B1S12P/B1S12N SCK pair. No other pins shall have differential termination installed on the PCB by default. Daughter boards should be designed to expect this termination resistor to exist whenever possible.

**The B1S12P/B1S12N SCK pair will have a 100\( \Omega \) resistor between them on the mother board.**

For some FPGA technologies it may be necessary to have the 100\( \Omega \) differential termination on the PCB, which is inherently “always on” and not selectable. This is required for example when implementing a memory interface running at +1.5V or below, while requiring the use of an LVDS clock to provide a reference frequency for the interface.

2.2.2 Signal Routing Requirements
This section details routing requirements for class 3 signals on the DINAR1 interface.

On the mother board, all signals shall be routed as 100\( \Omega \) differential pairs / 50\( \Omega \) single-ended signals. Loosely coupled routing is required. P to N length-matching must be done to within 10 mils. Each byte groups should be length-matched to within 25 mils. All signals across the interface shall be length-matched to within 100 mils on the mother board, matching as close as possible is recommended.

The daughter board has no specific signal routing requirements. Constraints for daughter board routing are application dependent and shall thus comply with any interface requirements, given the motherboard routing mentioned earlier.

2.3 Interface Clocking Requirements
This section describes the clocking requirements for class 3 signals on the DINAR1 interface.

There are two types of clocks on the interface, system clocks and local clocks. System clocks may be used to clock a synchronous across any (or all) banks on the DINAR1 interface with which they are
associated. Local clocks may be used to clock signals within the bank only. The clocks are defined as uni-directional, some are mother board inputs and some are daughter board inputs.

2.3.1 Mother Board Clock Inputs
There are two types of clock inputs on the mother board: system clocks and local clocks.

The mother board shall accept a system clock on any of the system clock pairs defined in the pin map (Figure 2). The clock can be differential or single-ended; single-ended clocks shall use the ‘P’ component of the differential pair. Any signaling level accepted by class 3 signals may be used.

The mother board shall accept a local clock on any of the local clock pairs defined in the pin map (Figure 2). The clock can be differential or single-ended; single-ended clocks shall use the ‘P’ component of the differential pair. Any signaling level accepted by class 3 signals may be used.

2.3.2 Daughter Board Single-Ended Clock Inputs
There are two types of clock inputs on the daughter board: system clocks and local clocks.

The daughter board shall select clock pairs as necessary for the interfaces that it implements and then accept a system clock on the system clock pairs defined in the pin map (Figure 2). The clock shall select and accept at least one signal standard that the motherboard is capable of driving.

The daughter board shall select clock pairs as necessary for the interfaces that it implements and then accept a local clock on the local clock pairs defined in the pin map (Figure 2). The clock shall select and accept at least one signal standard that the motherboard is capable of driving.

2.3.3 Clock Pin Selection
When selecting system clock pins for use as inputs on the mother board, it is highly recommended that pairs (100, 107), (196, 203), and (292, 299) be used first. When selecting local clock pins for use as inputs on the mother board, it is highly recommended that pairs (84, 91), (180, 187), and (276, 283) be used first.

Since system clock pin inputs have a superset of local clock pin input functionality, it is highly recommended that, as a second-tier decision criteria relative to the above, system clock inputs be used in preference for local clock inputs. For example, if up to four local clocks are required on bank 0, the pairs should be selected in the following order: ((100, 107), (84, 91), (22, 29), (38, 45)).

There are no pin selection guidelines for the daughter board interface.

2.4 Memory Interface Requirements
The DINAR1 interface makes provision for memory interfaces to be implemented on top of it. To this end, byte groups are defined, so that a memory controller can be implemented on the main board that utilizes memory ICs or modules hosted on the daughter board. There are some specific constraints that need to be adhered to when designing memory daughter boards that can be efficiently hosted by the main board.
2.4.1 Byte Group Pin Map

A pin map, denoting the byte groups in the DINAR1 interface, is given below. Byte groups are two columns wide each and are separated by dotted lines.

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>PWRGD</th>
<th>7</th>
<th>8</th>
<th>+5V</th>
<th>GROUND</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>PRSNT</th>
<th>14</th>
<th>PWRDN</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>17</td>
<td>18p</td>
<td>19</td>
<td>20p</td>
<td>21</td>
<td>22p</td>
<td>23</td>
<td>24p</td>
<td>25n</td>
<td>26</td>
<td>27n</td>
<td>28</td>
<td>29n</td>
<td>30</td>
<td>31n</td>
<td>VREF</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>34p</td>
<td>35</td>
<td>36p</td>
<td>37</td>
<td>38p</td>
<td>39</td>
<td>40p</td>
<td>41n</td>
<td>42</td>
<td>43n</td>
<td>44</td>
<td>45n</td>
<td>46</td>
<td>47n</td>
<td>48</td>
<td>49p</td>
<td></td>
</tr>
<tr>
<td>50p</td>
<td>51</td>
<td>52p</td>
<td>53</td>
<td>54p</td>
<td>55</td>
<td>56p</td>
<td>57n</td>
<td>58</td>
<td>59n</td>
<td>60</td>
<td>61n</td>
<td>62</td>
<td>63n</td>
<td>64</td>
<td>65p</td>
<td></td>
<td></td>
</tr>
<tr>
<td>66p</td>
<td>67</td>
<td>68p</td>
<td>69</td>
<td>70p</td>
<td>71</td>
<td>72p</td>
<td>73n</td>
<td>74</td>
<td>75n</td>
<td>76</td>
<td>77n</td>
<td>78</td>
<td>79n</td>
<td>80</td>
<td>81p</td>
<td></td>
<td></td>
</tr>
<tr>
<td>82p</td>
<td>83</td>
<td>84p</td>
<td>85</td>
<td>86p</td>
<td>87</td>
<td>88p</td>
<td>89n</td>
<td>90</td>
<td>91n</td>
<td>92</td>
<td>93n</td>
<td>94</td>
<td>95n</td>
<td>96</td>
<td>97p</td>
<td></td>
<td></td>
</tr>
<tr>
<td>98p</td>
<td>99</td>
<td>100p</td>
<td>101</td>
<td>102p</td>
<td>103</td>
<td>104p</td>
<td>105n</td>
<td>VREF</td>
<td>106</td>
<td>107n</td>
<td>108</td>
<td>109n</td>
<td>110</td>
<td>111n</td>
<td>112</td>
<td></td>
<td></td>
</tr>
<tr>
<td>113</td>
<td>114p</td>
<td>115</td>
<td>116p</td>
<td>117</td>
<td>118p</td>
<td>119</td>
<td>120p</td>
<td>121n</td>
<td>122</td>
<td>123n</td>
<td>124</td>
<td>125n</td>
<td>126</td>
<td>127n</td>
<td>VREF</td>
<td>128</td>
<td></td>
</tr>
<tr>
<td>129</td>
<td>130p</td>
<td>131</td>
<td>132p</td>
<td>133</td>
<td>134p</td>
<td>135</td>
<td>136p</td>
<td>137n</td>
<td>138</td>
<td>139n</td>
<td>140</td>
<td>141n</td>
<td>142</td>
<td>143n</td>
<td>144</td>
<td></td>
<td></td>
</tr>
<tr>
<td>145</td>
<td>146p</td>
<td>147</td>
<td>148p</td>
<td>149</td>
<td>150p</td>
<td>151</td>
<td>152p</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 2.4.2 Data vs Control Pin Placement

In general, data pins should be placed in banks 0 and 2. Control pins should be placed in bank 1.  

### 2.4.3 Clock Placement

If a reference clock is required, in general, it should be placed on system clock pair (196, 203).

---

Although this breaks interface encapsulation, best practices dictate that FPGA Design tools such as Xilinx Coregen Memory Interface Generator should be used to verify all planned memory interface pinouts for compatibility with main boards across the daughter card interface.
2.4.4 **Impedance Control Requirements**

Is it recommended that the VRP/VRN pins be used to calibrate the impedance of the mother board I/O pins when a high-speed memory interface is implemented across the DINAR1. At least one pair of VRP/VRN pins must be used per interface. It is recommended that the bank 1 pins be used preferentially since this allows “cascading” to the adjacent banks.

2.4.5 **Routing Requirements**

Routing requirements vary between memory interface types. When a memory daughter board is designed, the requirements for the interface must be met, taking into account the routing that is guaranteed by the mother board (section 2.2.2).

2.5 **Power Provision & Control Signals**

This section details power delivery and system-level control signals on the DINAR1 interface.

Three power rails are available across the DINAR1 interface header. The below schematic clipping shows the location of class 1 and 2 (power and control) signals on the DINAR1 mother board interface header schematic symbol:

![Schematic Clipping Demo](image)

*Figure 6 - Schematic Clipping Demonstrating Location of Class 1 and 2 Signals on DINAR1 Mother Board Header Schematic Symbol*

The +12V and +3.3V rails are sourced from the mother board. The $V_{CCO}$ rail is split up into several isolated sub-rails, one per bank; the $V_{CCO}$ pins are located on the schematic symbols with other class 3 pins. Each of the $V_{CCO}$ rails is provided by the daughter board, although they are biased by the mother board.

Four control signals are provided on the interface. The function of these signals is detailed in section 2.5.5.
2.5.1  +12V Rail
The +12V rail shall be driven by the mother board; it shall provide a voltage of +12V ± 10%. It is intended for use as an input voltage for switching power supplies. The mother board shall provide at least 2A on this rail; the daughter board shall draw no more than 2A.

+12V is guaranteed to come up before or with +3.3V.

It is recommended that a 5A or greater fuse be installed in-line on the daughter board for this rail.

2.5.2  +3.3V Rail
The +3.3V rail shall be driven by the mother board; it shall provide a voltage of +3.3V ± 5%. It is intended for use as an input voltage for linear drop-out power supplies. The mother board shall provide at least 3A on this rail; the daughter board shall draw no more than 3A.

+3.3V is guaranteed to come up after or with +12V.

It is recommended that a 5A or greater fuse be installed in-line on the daughter board for this rail.

2.5.3  V\text{CCO} Rail
The V\text{CCO} rails shall be driven by the daughter board. They are intended for use as a reference voltage for class 3 signals, and as a source voltage for I/O buffers on class 3 signals. The signals on each bank B0-B2 are referenced to the corresponding V\text{CCO} voltage, and the voltage rails are to be isolated on the mother board (although not necessarily on the daughter board). The V\text{CCO} rails may be referred to as V\text{CCO}_0 through V\text{CCO}_2 for interface banks 0 through 2 respectively.

The daughter board shall provide at least 1A of current per interface bank, increasing to 2A if HSTL or SSTL signaling is to be used. It is highly recommended that the daughter board connect together V\text{CCO} rails for banks 0 and 1.

The voltage on the V\text{CCO} rail shall be between +1.2V and +1.8V. The mother board shall provide low-current (500mA per bank) power supplies that bias the V\text{CCO} rails to +1.2V ±5%; these supplies shall shut down if a daughter board impresses a higher voltage on the V\text{CCO} rails.

V\text{CCO} shall not come up faster than +12V. V\text{CCO} shall not come up faster than +3.3V.

2.5.3.1  Power Sequencing Relative to V\text{CCO}
No class 3 shall be driven above V\text{CCO} + 0.3V by either mother board or daughter board. To meet this requirement it is recommended that both mother board and daughter board use V\text{CCO} as the V\text{CC} rail for their I/O buffers.

The daughter board must not drive V\text{CCO} power until the Power On (PWR\_ON) signal has been asserted. See section 2.5.5.4 for an explanation of this.

2.5.3.2  V\text{CCO} Requirements for Banks with No Connected Pins
If a daughter board does not connect any of the pins within an entire I/O bank, it may leave V\text{CCO} for that bank unconnected.
2.5.4 **Ground Pins**
There are many ground pins on the DINAR1 interface header. These serve as both as digital ground (i.e. signal return paths and digital power supply grounds) and chassis ground. They shall be connected to digital ground on both mother and daughter boards.

2.5.5 **Control Signals**
There are four control signals on the DINAR1 interface. These are used for power sequencing and interface management. Their purpose and associated requirements are described in this section.

2.5.5.1 **Driver and Pull-Up Requirements**
Most of the signals in this section specify the use of open-drain drivers and pull-ups. The requirements for these are specified below.

All open-drain drivers shall tolerate a voltage of up to +3.3V + 5% on their outputs, irrespective of the state of the daughter board power rails. They shall be able to sink at least 4mA at a V_{OL} of +0.45V.

All pull-ups shall be to +SEQ. They shall not provide current less than 100μA or in excess of 700μA when the signal they pull up is shorted to ground.

2.5.5.2 **Daughter Board Presence Detect**
Pin 13 of the interface, PRSNT#, is the daughter board presence detect. It is an active low signal that signals the presence of a daughter board to the mother board. It shall be either driven by an open-drain driver or shorted to ground on the daughter board. It shall be pulled to +SEQ on both mother board and daughter board, if the daughter board implements an open-drain driver (as opposed to a short to ground).

2.5.5.3 **Sequencing Power Supply**
The sequencing power supply pin, +SEQ, is a low-current auxiliary power supply that is to be used for powering sequencing circuitry. It may be provided by all end-points on the DINAR1 interface, both mother boards and daughter boards. It must be provided by the mother board.

The power supplies on this rail should tolerate V_{O} of +3.3V + 5%, regardless of their V_{IN} status. They should output a voltage of +2.5V ±10%, and be able to supply no less than 20mA of current. The power supply should start up with the input voltage of the system, typically +12V. The power supplies should not be damaged if their output is shorted to ground for an extended period of time.

All sequencing circuitry should be able to function off the voltage provided by the +SEQ pin.

2.5.5.4 **Power On**
The PWR_ON signal, pin 15, is an active-high signal that signals that the daughter board may power on its V_{CCO} power supplies. It is to be an open-drain output on the mother board, pulled high on both mother boards and daughter boards to +SEQ. Before this pin goes high, the daughter board may not drive the V_{CCO} supplies\(^7\).

\(^7\) Some feed-through is acceptable provided it does not exceed +0.7V.
2.5.5.5  **Power Good**  
The PWR_GD signal, pin 6, signals to the mother board that daughter board power supplies have stabilized. It is to be an open-drain output on the daughter board, pulled high on mother boards and daughter boards to +SEQ. It must be implemented on the daughter board. Its implementation on the mother board is optional; if it is not used, it should be pulled to +SEQ.

2.6  **Configuration Signals**  
This section describes the rules pertaining to class 5 “configuration” signals on the DINAR1 interface. The intent of these signals is to implement a serial configuration interface that can be used to program a daughter board hosted FPGA from the mother board.

2.6.1  **Configuration Signal Interface**  
The class 5 “configuration” signals form a sub-interface that is to some extent independent from the rest of the DINAR1 interface. The only non-class 5 signals that have relation to class 5 signals are PWR_ON, PWR_GD, and PRSTN#, which are described in section 2.5.5. The below diagram describes the configuration interface, which is comprised of the class 5 signals.

![Configuration Interface Diagram](image)

**Figure 7 - DINAR1 Configuration Sub-Interface**

The DINAR1 configuration sub-interface is designed to be compatible with both Xilinx “Slave Serial” and Altera “Passive Serial” configuration modes. These modes are defined in Xilinx UG470 and the Altera Straitx-5 Handbook respectively.

All class 5 signals are to be referenced to power supplies at +1.8V ±5%. Power supplies for the daughter board and for the mother board are intended to be separate. The daughter board power supply for the
configuration signals is referred to as $V_{CCO\_CFG\_DC}$, the mother board power supply for the configuration signals is referred to as $V_{CCO\_CFG\_MB}$.

Signal function is described in section 2.6.2. Signal levels are defined in 2.6.3. Power-on interface function and power supply sequencing is described in section 2.6.4.

### 2.6.2 Signal Description

This section describes the purpose and function of each of the class 5 signals.

#### 2.6.2.1 PROG_B

The PROG_B signal is intended an active-low reset for the daughter board FPGA. PROG_B will be pulled low with a 10kΩ resistor on the main board, and will be pulled to ground. The daughter board will pull the PROG_B signal high to $V_{CCO\_CFG\_DC}$ with a 470Ω resistor.

PROG_B is driven low or tri-stated by the mother board upon power-on. Once PWR_GD has been asserted, PROG_B will be tri-stated by the mother board. When the mother board initiates configuration, it shall pulse PROG_B low to clear the daughter board FPGA. PROG_B may never be driven high by the mother board, only tri-stated.

A daughter board not implementing the DINAR1 Configuration Interface may leave PROG_B floating or pull it low with a resistor.

#### 2.6.2.2 INIT_B

The INIT_B signal is intended to be used as a signal, driven by the daughter board, that the daughter board is ready to accept configuration. When the INIT_B signal is high, the mother board may configure the daughter board. It shall be pulled low with a 10kΩ resistor on the main board. The daughter board will pull the INIT_B signal high to $V_{CCO\_CFG\_DC}$ with a 470Ω resistor.

Daughter boards not implementing the DINAR1 Configuration Interface are recommended to connect the INIT_B signal to ground.

#### 2.6.2.3 CCLK

The CCLK signal is the clock for the serial configuration data. The mother board shall transmit CCLK; the daughter must should use CCLK to clock in data from the DIN pin on the rising edge. The signal is driven with a CMOS driver on the main board. It shall be pulled low with a 10kΩ resistor on the main board. It may be pulled low with a 10kΩ resistor on the daughter board.

A daughter board not implementing the DINAR1 Configuration Interface may leave CCLK floating or pull it low with a resistor.

#### 2.6.2.4 DIN

The DIN signal carries configuration data from the mother board to the daughter board. The mother board shall drive this signal with a CMOS driver. It shall be pulled low with a 10kΩ resistor on the main board. It may be pulled low with a 10kΩ resistor on the daughter board.
A daughter board not implementing the DINAR1 Configuration Interface may leave DIN floating or pull it low with a resistor.

2.6.2.5 **DONE**
The DONE signal is an active-high signal indicating that the daughter board FPGA has been configured successfully. It shall be pulled low with a 10kΩ resistor on the main board. It shall be either driven by the daughter board with a CMOS driver, or pulled to $V_{CCO_{CFG_{DC}}}$ with a resistor and driven with an open-drain buffer.

A daughter board not implementing the DINAR1 Configuration Interface may leave DONE floating or pull it low with a resistor.

2.6.3 **Signal Levels and Standards**
All signals are to use LVCMOS18 levels (see Table 1 for exact levels). The $V_{CC}$ power supply shall be $+1.8V \pm 5\%$ on both the mother board and the daughter board.

2.6.4 **Power Sequencing**
There are specific power-on sequencing requirements pertaining to the DINAR1 configuration sub-interface. Since the signals are powered by separate power supplies on the mother board and daughter board, care must be taken during power on so as not to damage the mother board or daughter board.

On the mother board, no signals may be driven high until the daughter board has asserted PWR_GD. PROG_B must be held low while PWR_GD is asserted. The mother board should not assert PWR_ON until $V_{CCO_{CFG_{MB}}}$ is within regulation.

The daughter board shall not power $V_{CCO_{CFG_{DC}}}$ until PWR_ON is asserted. The daughter board shall not assert PWR_GD until $V_{CCO_{CFG_{DC}}}$ is within regulation.

The mother board shall not initiate configuration until the following conditions are met:

1. PRSNT# is asserted
2. PWR_ON has been asserted
3. PWR_GD is asserted
4. INIT_B is high (allowed to float by daughter board)
3 Mechanical Requirements
This section will describe the mechanical requirements for the DINAR1 interface. The mechanical requirements include specifying the Samtec SEAM/SEAF connectors used in the interface, describing the board outline, and discussing system-level considerations.

3.1 Daughter Card Outline Definition
This section will detail the daughter card outlines designated for the DINAR1 interface. Two outline options are provided, full-length and half-length. All daughter boards implementing the DINAR1 interface shall comply with one of these two daughter board outlines. The full-length outline is 200mm long, while the half-length outline is 120mm long. The half-length outline and mounting holes fit completely into those specified for full-length cards. Thus, half-length daughter boards may be used in mother board positions designed for either half-length or full-length daughter boards. Full-length daughter boards may only be used in mother board positions designed for full-length mother boards. Note that in chassis applications, half-length daughter cards hosted in full-length slots may not reach the header aperture plate and thus access to the headers on daughter board may be restricted.

In general, it is recommended that main boards make allocation for full-length cards where possible to maximize compatibility with all daughter card form factors.

A daughter card implementing either the full or half-length outline option must cover the entire outline and implement all mounting holes. It is recommended that the mother board cover the entire daughter board outline and provide corresponding mounting holes. The mother board shall have matching mounting holes wherever the mother board overlaps a daughter board outline mounting hole.

Exceptions to the requirement to cover the entire outline may be made when an off-board connector placed on the board requires a cut-out or “notch” in the side of the board. In this case the daughter board outline may be resized as appropriate, provided that the connector is placed so as to mate with a chassis aperture plate placed in accordance with section Error! Reference source not found..

3.1.1 Daughter Board Outline, Full-Length
The following diagram describes the DINAR1 full-width daughter board outline. All full-length cards implementing the DINAR1_NS interface shall comply with this diagram, including all dimensions and mounting hole locations.
This edge may be touching the rear of the chassis

Note: Connector is mounted on SOLDER SIDE of PCB. This view is therefore looking THROUGH the PCB.

**Figure 8 - Illustration of DINAR1 Full-Length Daughter Card Outline**

Note: Holes to have 2.8mm drill, 5mm keepout, unplated
Figure 8 shows the full-length daughter card outline from the component side of the daughter card. Where the main board overlaps the daughter board outline, the main board shall have the corresponding set of mounting holes to accept either baseplate-mounted standoffs (for chassis applications) or mother board to daughter board standoffs (for non-chassis applications).

3.1.2 Daughter Board Outline, Half-Width
The following diagram describes the DINAR1 half-width daughter board outline. All half-width cards implementing the DINAR1 interface shall comply with this diagram, including all dimensions and mounting hole locations.

**Proposed Outline (Half-Length)**

This edge may be touching the rear of the chassis

*Note: Holes to have 2.8mm drill, 5mm keepout, unplated
Note: Connector is mounted on SOLDER SIDE of PCB. This view is therefore looking THROUGH the PCB.

**Figure 9 - Illustration of DINAR1 Half-Length Daughter Card Outline**
Figure 9 shows the half-width daughter card outline from the component side of the daughter card. Where the main board overlaps the daughter board outline, the main board shall have the corresponding set of mounting holes to accept either baseplate-mounted standoffs (for chassis applications) or mother board to daughter board standoffs (for non-chassis applications).

3.1.3 **Double-Width Layout Outline**
A double-width layout outline may be allowed for on a system level. Requirements for this outline are specified in section 3.3.5.

3.1.4 **Main Board Layout for DINAR1 Interface Compatibility**
Figure 8 and Figure 9 both illustrate daughter board outlines for the DINAR1 interface. These outline drawings are viewed from the component side of the daughter board, i.e. with the SEAM connector on the back. The mother board outline location and mounting holes should mirror the daughter board outline.

3.1.5 **Example Daughter Board Layouts**
This section features some example daughter board layouts, in both full-width and half-width outlines. This section does not contain any recommendations or requirements; it exists solely to illustrate how the DINAR1 interface daughter board outlines may be adapter for common use cases.

3.1.5.1 **+3.3V I/O Expansion Board**
The below diagram illustrates an example board layout for expansion of the system with +3.3V GPIO. The daughter board features a Kintex-7 part to handle voltage translation (as the Kintex-7 has numerous +3.3V-tolerant I/O pins).
3.2 Mezzanine Stack Description
This section will describe the mezzanine stack. Included will be a specification for the connectors used and drawings for mated connector systems.

3.2.1 Connector Specification
The DINAR1 interface shall use the Samtec SEARAY series of connectors.

Figure 10 - Example Layout for Full-Width Daughter Board for +3.3V GPIO Expansion
- The mother board shall use the **Samtec SEAF-40-05.0-S-10-2-A-K-TR** connector
  - DINI PID 3513
- The daughter board shall use the **Samtec SEAM-40-07.0-S-10-2-A-K-TR** connector.
  - DINI PID 3672

It is recommended that the mother board mount the SEAF connector on the component side. The daughter board shall always mount the SEAM connector on the solder side.

Each connector shall have a pair of mounting holes, used to secure the connectors together. The holes are to have a 2.8mm diameter drill, and a 5mm diameter keepout. The daughter board shall have unplated holes in the circuit board near the SEAM connector to allow the latching pins of the main board SEAF to pass through the daughter board PCB.

![Figure 11 - SEAM/SEAF Marketing Illustration](image)

#### 3.2.1.1 Mounting Hole Coverage and Attachment

All mounting holes in each outline shall be used to secure the boards together and possibly to a baseplate, if it is present in the system. If the mother board does not cover the extent of some of the outline and (necessarily) lacks the appropriate mounting holes, provisions shall be made to secure the non-covered mounting holes of the daughter board to a baseplate or similar supporting structure. Consider the following illustration:
In Figure 12, we see that the left-most mounting hole is “covered” by both mother board and daughter board. Here, we attach both mother board and daughter board together to the base plate, using a standoff/screw set. The right-most mounting hole is not covered by the mother board; the mother board’s right-most board edge terminates to the left to this hole. In this case, we use a standoff/spacer/screw set to attach the daughter board directly to the mother board. This application is described in more detail in section 3.2.3.

The daughter board must always fill the entire outline and hence shall implement all mounting holes called out in this specification. See section 3.1 for more information about daughter board outlines and mounting hole locations.

3.2.1.2 Connector, Alternate Orientation
Typically, the mother board SEAF connector should be placed on the component side of the mother board. For some applications, it may be desirable to place the mother board SEAF connector on the solder side of the circuit board. The daughter board connector should always be on the solder side of the daughter board. See sections 3.2.3 and 3.2.4.5 for more information on the Alternate Orientation for daughter board mounting.

3.2.2 Stack Illustration, Baseplate Used (Preferred Orientation)
The DINAR1 interface assumes that the mother board connector is mounted on the component side of the motherboard, while the daughter card SEAM connector is on the solder side of the daughter board. This is termed the “preferred” orientation. The proposed stack is illustrated below:
This section will detail the mechanical requirements of the DINAR1 interface with regards to the mezzanine-style stacking orientation when used with a baseplate.

### 3.2.2.1 Clearance Requirements

The main board shall have top side components no taller than 5.35mm where the daughter board outline overlaps the mother board. The main board is recommended to have thickness of 0.100". The DINAR1 interface makes no recommendations for component side component heights for main boards.

The daughter board shall have backside components (between the daughter board solder side and chassis baseplate) no taller than 4.00mm. The daughter board is recommended to have thickness of 0.062". All component-side parts on the daughter boards shall be shorter than 27mm for DINAR1 chassis applications.

It is recommended that the top surface of any components taller than 2mm be either electrically insulated or shorted to chassis ground (or equivalent, i.e. digital ground in most applications).

The chassis baseplate is required to have thickness of 0.047"; this corresponds to 18 gauge sheet metal.

### 3.2.2.2 Hardware Requirements, Main Board

It is required that the mainboard be attached to the baseplate using the combination of a ¼” spacer, 15/32” female-female standoff, and 5/8” screw, all threaded for 2-56 threads.

It is recommended that the standoffs be brass. A drawing of a standoff meeting these requirements is given below.
A ¼” threaded standoff with outside diameter of 3/16” tapped for 2-56 thread screws shall be used. It is recommended that the standoff be made of brass. A drawing of a standoff meeting these requirements is given below.
It is required that the baseplate be attached to the standoffs and spacers using 5/8” long screws, threaded with 2-56 threads. It is recommended that they be allen-head socket cap screws made of alloy steel plated with zinc. A drawing of a screw meeting these requirements is given below:

![Figure 16 - CAD Drawing of Example Main Board Screw for Chassis (Alternate) Applications](image)

It is required that a washer no thicker than 0.02” be placed between the screw head and the base plate, and also between the standoff in Figure 14 and the main board PCB. A drawing of a washer meeting these requirements is given below:

![Figure 17 - CAD Drawing of Example Baseplate Washer for Chassis (Alternate) Applications](image)
3.2.2.3 **Hardware Requirements, Daughter Board**

It is required that the daughter board be attached to the base plate using ¼” long, 2-56 threaded screws. It is recommended that allen-head socket cap screws, made of alloy steel plated with zinc, be employed. A drawing of a screw meeting these requirements is given below:

![CAD Drawing of Example Daughter Board Screw for Chassis (Alternate) Applications](image1)

Figure 18 - CAD Drawing of Example Daughter Board Screw for Chassis (Alternate) Applications

It is required that a washer no thicker than 0.02” be placed between the screw head and the component side of the PCB. A drawing of a washer meeting these requirements is given below.

![CAD Drawing of Example Daughter Board Washer for Chassis (Alternate) Applications](image2)

Figure 19 - CAD Drawing of Example Daughter Board Washer for Chassis (Alternate) Applications
3.2.2.4 Recommended Hardware Part Numbers
Hardware meeting the requirements of sections 3.2.3.2 and 3.2.3.3 can be ordered from McMaster-Carr. Reference the following part numbers:

<table>
<thead>
<tr>
<th>Part Description</th>
<th>McMaster-Carr Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Board Standoff</td>
<td>90308A008</td>
</tr>
<tr>
<td>Main Board Screw</td>
<td>90128A054</td>
</tr>
<tr>
<td>Baseplate Washer</td>
<td>90945A705</td>
</tr>
<tr>
<td>Main Board Standoff (bottom)</td>
<td>90308A103</td>
</tr>
<tr>
<td>Daughter Board Screw</td>
<td>90128A042</td>
</tr>
<tr>
<td>Daughter Board Washer</td>
<td>90945A705</td>
</tr>
</tbody>
</table>

3.2.2.5 Mechanical Assembly Illustration
The following is a mechanical assembly illustration for the standoff and board mezzanine stack. This illustration details the stack for chassis and baseplate-mounted applications.

Available in high resolution on PDF.

3.2.3 Stack Illustration, Baseplate Used (Alternate Orientation)
The DINAR1 allows for the SEAF mother board connector to be mounted on the solder side of the mother board. This is termed the “alternate” orientation. The DINAR1 alternate stack for chassis applications assumes a baseplate on the opposite side of the mother board. It is recommended that the mother board cover the entire daughter board outline, so that the two boards may be mated together. If this is not possible, the non-covered daughter board mounting holes must be secured to the baseplate directly.
The proposed stack for this alternate orientation is illustrated below.

Proposed Stack (Chassis, Alternate)

Figure 21 - Illustration of Proposed Stack for DINAR1 in Chassis (Alternate) Applications

This section will detail the mechanical requirements of the DINAR1 interface with regards to the mezzanine-style stacking orientation.

3.2.3.1 Clearance Requirements
The main board shall have backside components (between the main board solder side and chassis baseplate) no taller than 5.35mm. The main board is recommended to have thickness of 0.100”. The DINAR1 interface makes no recommendations for component side component heights for main boards.

The daughter board shall have backside components (between the daughter board solder side and chassis baseplate) no taller than 4.00mm. The daughter board is recommended to have thickness of 0.062”. All component-side parts on the daughter boards shall be shorter than 27mm for DINAR1 chassis applications.

It is recommended that the top surface of any components taller than 2mm be either electrically insulated or shorted to chassis ground (or equivalent, i.e. digital ground in most applications).

The chassis baseplate is required to have thickness of 0.047”; this corresponds to 18 gauge sheet metal.

3.2.3.2 Hardware Requirements, Main Board
It is required that the mainboard be attached to the baseplate using ¼” tall, 3/16” hex outside dimension, 2-56 threaded, male-female standoffs. It is recommended that these standoffs be brass. A drawing of a standoff meeting these requirements is given below.
It is required that the main board be attached to the standoffs using ¼” long screws, threaded with 2-56 threads. It is recommended that they be allen-head socket cap screws, made of alloy steel, plated with zinc. A drawing of a screw meeting these requirements is given below:

It is required that a washer no thicker than 0.02” be placed between the screw head and the component side of the PCB. A drawing of a washer meeting these requirements is given below.
3.2.3.3 Hardware Requirements, Daughter Board, Overlapping Main Board

For applications where a main board overlaps the daughter board outline, it is required that the daughter board be attached to the base plate using 3/16” tall, 3/16” male-female 2-56 threaded standoffs. It is recommended that these be brass standoffs. A standoff meeting these requirements is depicted below:

It is required that the daughter board be attached to the standoffs using 3/16” hex nuts with 2-56 threading. It is required that the nut be no taller than 1/16”. A drawing of a nut meeting these requirements is given below:
It is required that a washer no thicker than 0.02” be placed between the daughter board nut and the component side of the PCB. A drawing of a washer meeting these requirements is given below.

3.2.3.4 Hardware Requirements, Daughter Board, Non-Overlapping Main Board
For applications where a main board does not overlap the daughter board outline, it is required that the daughter board be attached to the base plate using a combination of a 5/8” 2-56 threaded screw and a 3/16” 2-56 threaded Female-Female standoff.
It is required that the daughter board be attached to the standoffs using 3/16" hex nuts with 2-56 threading. It is required that the nut be no taller than 1/16". A drawing of a nut meeting these requirements is given below:
It is required that a washer no thicker than 0.02” be placed between the daughter board nut and the component side of the PCB. A drawing of a washer meeting these requirements is given below.

3.2.3.5 Recommended Hardware Part Numbers

Hardware meeting the requirements of sections 3.2.3.2 and 3.2.3.3 can be ordered from McMaster-Carr. Reference the following part numbers:

Table 4 - Recommended Chassis (Preferred) Mounting Hardware, McMaster-Carr Part Numbers
### Part Description

<table>
<thead>
<tr>
<th>Part Description</th>
<th>McMaster-Carr Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Board Standoff</td>
<td>92700A211</td>
</tr>
<tr>
<td>Main Board Screw</td>
<td>90128A042</td>
</tr>
<tr>
<td>Main Board Washer</td>
<td>90945A705</td>
</tr>
<tr>
<td>Daughter Board Standoff  (M-F)</td>
<td>92700A512</td>
</tr>
<tr>
<td>Daughter Board Standoff  (F-F)</td>
<td>90308A102</td>
</tr>
<tr>
<td>Daughter Board Nut</td>
<td>96537A110</td>
</tr>
<tr>
<td>Daughter Board Washer</td>
<td>90945A705</td>
</tr>
</tbody>
</table>

#### 3.2.3.6 Mechanical Assembly Illustration

The following is a mechanical assembly illustration for the standoff and board mezzanine stack. This illustration details the stack for chassis and baseplate-mounted applications. This drawing assumes that both main board and daughter board are being mounted to the baseplate using a corresponding mounting hole location.

**Standoff Mechanical Assembly, Chassis Alternate**

Pro Tip: Apply Valvoline VV986 to screw thread tip before installing into standoff

Pro Tip: Apply Permatex 24200 Threadlock Between MB Standoffs

Assemble together stack
Recommended order:
1. Standoffs to baseplate
2. Mother Board PCB to standoffs
3. Daughter board PCB to standoffs

Figure 32 - Board Mezzanine Stack Assembly Illustration (Chassis Applications, Alternate)

If there is no corresponding mounting hole in the main board due to a lack of overlap between the mainboard and daughter board outlines, the mounting procedure is simplified. Hardware should be used from section 3.2.3.4 and installed first onto the base plate, and then onto the daughter board.

#### 3.2.4 Stack Illustration, No Baseplate (Non-Chassis Applications)

The DINAR1 interface specification assumes that the SEAF connector is mounted on the top side of the mother board and the SEAM connector on the solder side of the daughter board; this is termed the “preferred” orientation. The DINAR1 interface stack assumes no baseplate for chassis-free applications. The proposed stack for chassis-free setups is illustrated below:
This section will detail the mechanical requirements of the DINAR1 interface with regards to the mezzanine-style stacking orientation.

3.2.4.1 Clearance Requirements
The main board shall have top side components (between the main board component side and daughter board) no taller than 5.35mm where the daughter board outline overlaps the main board. The main board is recommended to have thickness of 0.100”.

The daughter board shall have backside components (between the daughter board solder side and chassis baseplate) no taller than 4.00mm. The daughter board is recommended to have thickness of 0.062”. The DINAR1 interface makes no recommendations for component side component heights for daughter boards in non-chassis applications.

It is recommended that the top surface of any components taller than 2mm be either electrically insulated or shorted to digital ground.

3.2.4.2 Hardware Requirements
It is required that the mainboard be attached to the daughter board 3/16” hex, 15/32” long female-female 2-56-threaded standoffs. It is recommended that these standoffs be brass. A drawing of a standoff meeting these requirements is given below.
It is required that the main board and the daughter board be attached to the standoffs using ¼" long screws, threaded with 2-56 threads. It is recommended that they be allen-head socket cap screws made of alloy steel with zinc plating. A drawing of a screw meeting these requirements is given below:
It is required that a washer no thicker than 0.02” be placed between the screw head and the component side of the PCB. A drawing of a washer meeting these requirements is given below.

3.2.4.3 Recommended Hardware Part Numbers

Hardware meeting the requirements of section 3.2.4.2 can be ordered from McMaster-Carr. Reference the following part numbers:

<table>
<thead>
<tr>
<th>Part Description</th>
<th>McMaster-Carr Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board Standoff</td>
<td>90308A008</td>
</tr>
<tr>
<td>Screw</td>
<td>90128A042</td>
</tr>
<tr>
<td>Washer</td>
<td>90945A705</td>
</tr>
</tbody>
</table>

3.2.4.4 Mechanical Assembly Illustration

The following is a mechanical assembly illustration for the standoff and board mezzanine stack. This illustration details the stack for chassis-free applications.
Standoff Mechanical Assembly, Chassis-Free

Assemble together stack
Recommended order:
1. Mother Board PCB to standoff
2. Daughter board PCB to standoff

![Figure 37 - Board Mezzanine Stack Assembly Illustration (Chassis-free Applications)](image)

3.2.4.5 Alternate Orientation
The DINAR1 specification provides for an “alternate” orientation of the non-chassis mother-daughter board mounting. Here, the solder side of the mother board faces the solder side of the daughter board. The only difference is that the mother board shall have no components taller than 5.35mm within the area of the daughter board outline on the solder side of the main board. Otherwise the same hardware can be used as for the preferred mounting orientation.

![Proposed Stack (Chassis-Free, Alternate)](image)

3.3 Chassis and System-Level Requirements for DINAR1 Implementations
This section will describe chassis and system requirements for boards implementing the DINAR1 interface. In particular, the location of the chassis rear panel and connector placement guidelines will be described. Power dissipation requirements will also be addressed.

Most of this section may be ignored for chassis-free DINAR1 implementations.

3.3.1 Rear panel location
The DINAR1 specification assumes that the chassis rear panel is located at the east end of the board outlines (see Figure 8, Figure 9) and provide an opening for various power and signal connectors coming off of the DINAR1 daughter board. The chassis rear panel shall be placed 2mm (nominal) away from the edge of the PCB. The chassis front panel itself shall have thickness 0.036”. The opening for connectors shall be 27mm tall and extend along the east edge of the DINAR1 daughter card outline, to within 6.5mm of the north and south ends of the edge.
Any connector placement on a DINAR1 daughter board shall tolerance a front plate placement tolerance of +1mm, -0.5mm from the nominal measurements given in the previous paragraph. The below drawing depicts the placement of the front panel relative to the daughter board PCB.

**Rear Panel Interface (Chassis Applications)**

**Side View**

![Side View Diagram](image)

**Rear Panel Interface (Chassis Applications)**

**Top View**

![Top View Diagram](image)
3.3.2 **Rear panel connector opening**
The rear panel connector opening, termed the header aperture, shall be centered on the DINAR1 daughter board east edge. It shall be 77mm wide and 33mm tall\(^8\); the maximum opening area on the aperture plate is 74mm by 27mm with 1.5mm padding from the bottom, left, and right edges of the aperture area. The below drawings depict the header aperture plate, including the connector opening dimensions.

![Header Aperture Plate, Including Rear-Panel Opening (Front View)](image)

**Figure 41 - Header Aperture Plate, Including Rear-Panel Opening (Front View)**

The header aperture plate shall attach to the main chassis front plate with four \(\frac{\mu}{4}\) 2-56 screws, as in the above drawings. See Figure 23 for an illustration of a screw meeting these requirements. A washer shall also be employed, see Figure 24 for a washer that meets these requirements.

**Figure 42 - Header Aperture Plate (Top View)**

The header aperture plate shall attach to the main chassis front plate with four \(\frac{\mu}{4}\) 2-56 screws, as in the above drawings. See Figure 23 for an illustration of a screw meeting these requirements. A washer shall also be employed, see Figure 24 for a washer that meets these requirements.

3.3.3 **Daughter Board Component Height Limitation**
In section 3.2 we define a daughter card solder side component height limitations. The daughter board component side height limit shall be 27mm. It is recommended that any components taller than 4mm have their tops be either insulated or shorted to digital ground.

---

\(^8\) Note the vertical asymmetry in the panel vs chassis aperture placement; this is for ease of assembly as it gives additional room to aid the mating of the SEAM/SEAF connector pair.
3.3.4 **Daughter Board Spacing**
Adjacent daughter board positions shall be spaced at exactly 91mm center to center.

3.3.5 **Double-Wide Daughter Boards**
Two adjacent mother board positions, both either half-length or full-length, may be occupied by a single “double wide” daughter board.

Physically, the daughter board shall assume spacing as defined in 3.3.4 and shall take up the outlines of both boards, including the space between the two positions. All mounting holes within both outlines will be implemented.

Electrically, the daughter board will treat the two DINAR1 connectors as separate interfaces. +12V and +3.3V power rails shall remain isolated; the daughter board may not connect them together. +SEQ must remain isolated. All control signals must be implemented independently. V_{CCO} rails may be connected together on the daughter board; in this case, the daughter board must wait for both interfaces to assert PWR_ON before bringing up V_{CCO}. The double wide daughter board must not make any assumptions regarding the behavior of the power rails on one interface relative to the other.

**Proposed Outline (Double-Wide, Half-Length)**

![Diagram of Double-Wide Board Outline](image-url)

*Note: Connector is mounted on SOLDER SIDE of PCB. This view is therefore looking THROUGH the PCB.*

*Figure 43 - Illustration of Double-Wide Board Outline*
For double-wide daughter boards, it is required that electrical resources on DINAR1 Interface #1 be used first, before using resources on Interface #2. Unused electrical resources (unconnected power rails or signals) should be dealt with in accordance to the rules laid out in section 2.1.2.

### 3.3.6 Daughter Board Cabling
The system should make provisions to have multiple daughter board positions (possibly on different systems) to be connected together using a Samtec cable. Although custom specification and assembly of a cable will be required, assuming the rest of this specification is followed, there should be no other special considerations required for inter-system cabling to work.

### 3.3.7 Power Dissipation
The system design shall make provision for the daughter card to dissipate the maximum rated power that the DINAR1 interface provides via the Class 1 Power pins (section 2.5). Any additional power dissipation on the card, made possible (for example) through an external power header, is not accounted for by the system-level provisions of the DINAR1 specification.

The chassis shall provide an ambient air temperature of no warmer than 50°C. There is no minimum chassis airflow guaranteed for the DINAR1 daughter board.