DNSEAM_NS

High-Speed Serial I/O Expansion Interface Specification

Revision 1.8

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Last Updated 2014-03-19, A. Sikes
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1 Overview
This document describes the DNSEAM_NS high-speed I/O expansion interface. Mechanically, this interface is comprised of a single mother board and one or more I/O expansion daughter boards, mounted in a mezzanine fashion. Provisions are made to allow the interface to work with or without a chassis. Electrically, the interface is comprised of a number of high-speed serial signals, reference clocks, some lower-speed sideband connections, and power distribution.

The goal of the DNSEAM_NS specification is to specify a flexible, compact, and modular expansion interface that can be used to adapt the high-speed serial transceivers available on contemporary FPGAs to a variety of High-Speed Serial connector and interface types. The principal use model is to interface a Dini Group ASIC emulation mother board, which itself hosts FPGAs with multi-gigabit transceivers, to an I/O expansion daughter card, the latter having interfaces such as SFP+, PCI Express Cable, or SMA connectors. This approach can be employed to “break out” the high density DNSEAM_NS interface header to a wide range of commonly used High-Speed Serial connector types.

The DNSEAM_NS interface features two pinout alternatives, the Full(y Populated) pinout, termed DNSEAM_NS, and the Reduced pinout, termed DNSEAM_NS-R. The Full pinout is a superset of the Reduced pinout. Compatibility between the two is driven by the mother board. A Full pinout mother board can host either Full or Reduced daughter boards. A Reduced pinout mother board can only host Reduced daughter boards. There are no mechanical differences between the Full and Reduced pinout options, the only difference is how many electrical signals are connected. Section 2.1 clarifies the pinout options.

The DNSEAM_NS interface allows for two physical outline options, the Full-Width outline and the Half-Width outline. Compatibility between the two is driven by the mother board. A Full-Width mother board position can host either Full or Half-Width daughter boards. A Half-Width mother board position can only host Half-Width daughter boards. There are no electrical differences between the Full-Width and Half-Width outline options. The only difference is the physical size of the daughter board and the space allowance made by the mother board. Section 3.1 describes the physical outline options.

The DNSEAM_NS interface is used on several Dini Group boards including many Dini Group Xilinx 7-series ASIC emulation products. It is also designed to be backwards-compatible with daughter boards featuring the Virtex-6 DNSEAM interface, although specific compatibility must be verified on a case-by-case basis.

1.1 Other Files
This specification makes reference to several files and drawings. They are enumerated here

1. mechanical_drawings.pdf – an annotated set of drawings describing the DNSEAM_NS daughtercard form factor.
1.2 Terminology & Style
A variety of terminology is used throughout this document. Some of it has very specific meaning.

The phrases are to/shall/required/must state hard requirements for all cards implementing the DNSEAM_NS interface. The words highly recommended denote characteristics that are not hard requirements, but should be implemented where possible and are likely to become requirements in future major revisions of the DNSEAM_NS specification. The word recommended denotes characteristics that are not hard requirements nor likely to become such, but should be implemented where reasonable.

The terms “mother board,” “main board,” and “host” are used interchangeably, and refer to the FPGA-based Dini Group ASIC emulation board. The term “daughter board” or “parasite” refers to the smaller mezzanine board that contains the break-out High-Speed Serial connectors.

1.3 Revision History

0.1 – 2012-03-22, I. Yulaev
1. Initial Revision

0.2 – 2012-03-28, I. Yulaev
1. Added Reduced pinout option to DNSEAM_NS spec. Differentiated this pinout from the old option by terming the old pinout the “Full” pinout.
2. Added section 2.1.2.4 to make association between groups 2-4 subgroup 1 signals explicit, same for subgroup 2.
3. Added “alternate” orientation, where SEAM connector is mounted on mother board top side. This pertains mostly to sections 3.2.3 and 3.2.4.5.
4. Re-drew header pinout, Figure 1 and Figure 2
5. Schematic symbol updated (Figure 3)
6. Made use of REFCLK_A0 and REFCLK_B0 highly recommended, vs REFCLK_A1 and REFCLK_B1. Section 2.1.2.5.
7. Defined directionality of LVDS pairs in group 4 signals.
8. Made it explicit that daughter board mounting holes be attached to something. See section 3.2.1.1.
9. Added SEAF connector to Figure 50.
10. Made zinc plating recommended for all screws in section 3.
11. Increased current rating on +3.3V rail to 6A and on +12V rail to 4A (section 2.5)

0.3 – 2012-03-28, I. Yulaev
1. Various minor edits

0.4 – 2012-04-01, I. Yulaev
1. Added requirement of bonding ability for DNSEAM_NS xvcrs, see 2.1.2.3
2. Changed specification name to DNSEAM_NS
3. Added example layout for SFP+ cards, PCIe 8-lane connectors, SATA connectors, HDMI & DisplayPort, others
4. Moved daughter card outline section to beginning of section 3
5. Changed pinmap colors in section 2.1
6. Renamed groups 2-4 subgroup names from numeric (HSS1, HSS2, ...) to alphabetic (HSS-A, HSS-B) convention
7. Required that SB-A/RCK-A be used with HSS-A when possible, as with subgroups B. See 2.1.2.4
8. Changed VCCO specification to allow VCCO to go down to +1.2V, support for this is highly recommended. See section 2.5.3
9. Changed requirement for unused signals in section 2.1.2 to float rather than ground unused signals.
10. Schematic symbol and clippings in section 2.1 changed to reflect changes to specification, as detailed above
11. Section 2.5.3.1 changed to necessitate that signals not be driven above VCCO + 0.3V during power up.
12. Marked pin 1 in connector drawings, Figure 24, Figure 25. Also fixed daughter board connector drawing outline.
13. ¼” spacer in chassis alternate application should now be threaded. See section 3.2.3.
14. Daughter board outline changed slightly to align east-center mounting hole with south-most SEAM/SEAF connector mounting hole, see Figure 11, Figure 12
15. Added daughter board component height limitation (section 3.3.3)

0.5 – 2012-04-01 I. Yulaev
1. Added description of full-width and half-width physical outline options to section 1

1.0 – 2012-04-09 I. Yulaev
1. Obtained marketing sign-off. Upgraded to major revision 1. No notable changes.

1.1 – 2012-05-08 I. Yulaev
1. Added Dini interal PID for mother board connector to section 3.2.1

1.2 – 2012-06-22 I. Yulaev
1. Specified that the right edge of boards does not literally touch the faceplate, just faces it (section 3.1)
2. Added notes about exception in daughter card outline requirement, allowing for notches in the connector-facing edge when high-speed off board connectors require them (3.1)

1.3 – 2012-09-06 I. Yulaev
1. Revised drawings in sections 3.3.1 and 3.3.2 to reflect larger chassis aperture and 2mm spacing between DNSEAM_NS board edge and chassis panel.
2. Simplified design for header aperture place, Figure 52 and Figure 53.
3. Renamed “bulkhead” to “aperture” in section 3.3.

1.4 – 2012-10-19 I. Yulaev
1. Updated figures 51 and 52 for 1mm reduced width aperture.

1.5 – 2012-11-05 I. Yulaev
   1. Added pin 1 location to Figure 11, Figure 12

1.6 – 2013-08-21 N. Harder
   1. Fixed hole locations on many diagrams to match the first drawing in the document which was correctly labeled.

1.7 – 2013-10-28 N. Harder
   1. Fixed the Dini PID numbers for the SEAM and SEAF connectors in section 3.2.1.

1.8 – 2014-03-19 A. Sikes
   1. Corrected Figures 1 and 2: Pins 58 and 60 changed from “p” to “n”; pins 66 and 68 changed from “n” to “p”; pins 3, 5, 7, 25 and 55 had the wrong pin numbers..

1.4 Contact
For questions or comments regarding the interface specification, contact support@dinigroup.com.
2 Electrical Requirements

This section will define electrical requirements for the DNSEAM_NS interface. Enumerated will be requirements for signals, including signaling standards and routing requirements, as well as description of the logical interface requirements such as synchronous I/O timing information. Also in this section non-signal electrical requirements, i.e. power distribution, will be described.

2.1 Signal and Pinout Description

A pinout of the DNSEAM_NS interface header, using the FULL header pinout option, is given below. Pin numbers follow the SEAM/SEAF pin numbering convention. All pin numbers ending with ‘p’ represent the true component of a differential signal. All pin numbers ending with ‘n’ represent the complementary component of a differential signal.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
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<tr>
<td>3</td>
<td>+3.3V</td>
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<tr>
<td>4</td>
<td>+12V</td>
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<tr>
<td>5</td>
<td>+12V</td>
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<td>GROUND</td>
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<td>RX</td>
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<td>RX (2)</td>
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<td>TX</td>
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<td>106</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>107</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>108</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>109</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>110</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>111</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>112</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>113</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>114</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>115</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>116</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>117</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>118</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>119</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>120</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>121</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>122</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>123</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>124</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>125</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>126</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>127</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>128</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>129</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>130</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>131</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>132</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>133</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>134</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>135</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>136</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>137</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>138</td>
<td>1.3.3V</td>
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<tr>
<td>139</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>140</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>141</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>142</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>143</td>
<td>1.3.3V</td>
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<tr>
<td>144</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>145</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>146</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>147</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>148</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>149</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>150</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>151</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>152</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>153</td>
<td>1.3.3V</td>
</tr>
<tr>
<td>154</td>
<td>+12V</td>
</tr>
<tr>
<td>155</td>
<td>+12V</td>
</tr>
<tr>
<td>156</td>
<td>+12V</td>
</tr>
<tr>
<td>157</td>
<td>+12V</td>
</tr>
<tr>
<td>158</td>
<td>+12V</td>
</tr>
<tr>
<td>159</td>
<td>+12V</td>
</tr>
<tr>
<td>160</td>
<td>+12V</td>
</tr>
</tbody>
</table>

Figure 1 - DNSEAM_NS Interface Header Pinout, FULL Option

Notes:
1. RX, TX labels are relative to mother board.
2. Bold text indicates CC pin on MOTHER BOARD. Italic text indicates CC pin on DAUGHTER BOARD.
The pinmap for a header implementing the Reduced pinout option is given below.

![Figure 2 - DNSEAM_NS Interface Header Pinout, REDUCED Option](image)

The below figure shows the schematic symbol for the DNSEAM_NS mother board header (nominally Samtec SEAM-20-07.0-S-08-2-A-K-TR, see section 3.2.1). The daughter board header symbol is identical. Some annotation within the symbol is provided; this annotation will be clarified later in this document.
Figure 3 - DNSEAM_NS Mother Board Header Schematic Symbol
2.1.1 Signal Group Definition
This section will group the signals into signal groups, describe the function of each group, and define terminology for them. The signal groups are enumerated below. Note that sections 2.1 through 2.4 make minimal mention of signal group 1, “power” pins. These are specified in section 2.5.

2.1.1.1 Group 1 – Power
The Power pins include \( V_{CCO} \), +3.3V, and +12V.

2.1.1.2 Group 2 – High-Speed Serial
These pins are labeled RX and TX in Figure 1. These are high-speed differential pairs designated for compatibility with multi-gigabit signaling standards. Pins labeled RX are inputs to the transceivers on the mother board. Pins labeled TX are outputs of the transceivers on the mother board. The High-Speed Serial pins are split into two sub-groups, HSS-A and HSS-B. HSS-A is comprised of pins \{34, 42, 10, 18, 36, 44, 12, 20, 66, 58, 14, 22, 68, 60, 38, 46\}. HSS-B is comprised of pins \{127, 119, 151, 143, 125, 117, 149, 141, 103, 95, 147, 139, 101, 93, 123, 115\}.

On Reduced pinout daughter boards, only HSS-A is available.

2.1.1.3 Group 3 – REFCLK
These pins are designated specifically to provide reference clock frequencies to the mother board transceivers. They are differential inputs to the mother board. REFCLK signals are comprised of two sub-groups, RCK-A and RCK-B. RCK-A is comprised of pins \{16, 24, 40, 48\}. RCK-B is comprised of pins \{145, 137, 121, 113\}.

On Reduced pinout daughter boards, only RCK-A is available.

2.1.1.4 Group 4 – Sideband I/O
These pins are labeled SIGNAL in the above diagram. They are separated into two sub-groups, SB-A and SB-B. SB-A consists of pins \{81, 82, 83, 89, 91, 97, 98, 99\}. SB-B consists of pins \{62, 63, 64, 70, 72, 78, 79, 80\}. In LVDS mode only these have defined directionality, as per the diagram. Pins labeled RX are inputs to the transceivers on the mother board. Pins labeled TX are outputs from the transceivers on the mother board.

On Reduced pinout daughter boards, only SB-A is available.

2.1.2 Signal Connection Requirements

2.1.2.1 Signal Connection Requirement for Full Interfaces
The mainboard that implements the Full pinout option shall have all of the signals connected up appropriately. The daughter board is not required to connect all signals from groups 2 through 4; unused signals shall be left floating on the daughter card.

2.1.2.2 Signal Connection Requirements for Reduced Interfaces
A main board that implements the Reduced pinout option shall have all signals in Group 2 HSS-A, Group 3 RCK-A, and Group 4 SB-A connected appropriately. Signals from subgroup B of groups 2 through 4 shall be left floating.
The daughter board is not required to connect all signals from groups 2 through 4 subgroups A; unused signals from these subgroups shall be left floating on the daughter card. Signals from subgroup B of groups 2 through 4 shall be left floating.

2.1.2.3 Transceiver Bonding Requirements
On a motherboard implementing a Full pinout option interface, all eight channels shall have the capability of being bonded. Also, each Group 1 subgroup shall have the capability of being bonded. On a motherboard implementing a Reduced pinout option interface, all four channels shall have the capability of being bonded.

See section 2.4.1.2 for clocking recommendations for bonded transceivers.

2.1.2.4 Signal Group Association
Group 2 subgroup HSS-A is associated with Group 3 subgroup RCK-A and Group 4 subgroup SB-A. Therefore, it is required that daughter boards using HSS-A to implement an interface use signals in RCK-A and SB-A for this same interface, if at all possible. The same is true for Group 2 subgroup HSS-B, Group 3 subgroup RCK-B and Group 4 subgroup SB-B. This requirement aids in degradation if a non-Reduced daughter card is plugged into a DNSEAM_NS-R (Reduced connector format) main board.

2.1.2.5 REFCLK Connection Recommendations
It is highly recommended that the daughter board make use of REFCLK_A0 and REFCLK_B0 before making use of REFCLK_A1 and REFCLK_B1.

2.1.3 Reserved Pins
Pins 73, 84, 77, 88 are reserved for future use. Both the mother board and daughter board shall make provisions to tolerate any voltage between GND and Vcco on these pins.

2.2 Signaling Standards, Performance, and Level Tolerance
This section defines the signaling standards, level tolerance, and performance characteristics of signal groups 2-4, i.e. non-power pins.

2.2.1 Signaling Standards for High-Speed Serial Signals
This section defines the signaling standards applicable to group 2, “High-Speed Serial” signals.

RX signals, which are differential inputs on the mother board, shall tolerate single-ended VIN between -0.2V and +1.2V. The input differential swing, measured as the difference between P and N when P is high and N is low and when N is high and P is low, shall be no greater than 2000mV.

The below figure clarifies the measurements of differential peak-to-peak swing.¹

¹ Taken from Figure 2 of Xilinx DS183, “Virtex-7 Data Sheet”, v1.3 dated February 13, 2012
The following schematic clipping shows the location of these signals on the DNSEAM_NS mother board interface header schematic symbol:
TX signals, which are differential outputs on the mother board, shall have a common mode of \(+1.2- (\text{seV}_{PP}/2)\), where \(\text{seV}_{PP}\) is the single-ended output swing of the mother board.\(^2\)

d\(V_{PP}\) (which is \(\text{seV}_{PP} \times 2\)) is typically configurable on the mother board transceiver; it shall be at most 1000mV.

The main board shall implement 100Ω differential termination for the RX signal inputs. The main board shall re-bias the signals to a common mode that it can accept.

Neither the RX nor TX signals shall have AC coupling capacitors on the main board. All AC coupling shall be implemented by the daughter board as governed by signal standard, protocol, or application-specific implementation.

The DNSEAM_NS specification does not specify any performance requirements for group 2 signals. Performance requirements are dependent on the protocol and line rate in use, the capabilities of the mother board transceivers, the SEAM/SEAF header pair, and the daughter board design. Specifying these is outside of the scope of the DNSEAM_NS interface.

### 2.2.2 Signaling Standards for REFCLK Signals

This section defines the signaling standards applicable to group 3, “REFCLK” signals. These signals are differential-pair reference clock frequency carriers provided to the mother board (i.e. differential clock inputs on the mother board) by the daughter board. The below schematic clipping shows the location of these signals on the DNSEAM_NS mother board interface header schematic symbol:

\(^2\) Taken from Figure 1 of Xilinx DS183, “Virtex-7 Data Sheet”, v1.3 dated February 13, 2012
REFCLK signals shall have in-line AC coupling capacitors of between 0.1µF and 4.7µF on the motherboard. 100Ω differential termination for these signals shall be provided on the motherboard.

REFCLK signals shall have dV_{pp} between 250mV to 2000mV. It is highly recommended that the daughter board be designed such that a clock generator capable of outputting a differential clock with dV_{pp} of at least 600mV could be retrofitted into the daughter board assembly.

The DNSEAM_NS specification does not specify any performance requirements for group 3 signals. Performance requirements are dependent on the capabilities and requirements of the motherboard transceiver REFCLK inputs, the SEAM/SEAF header pair, and the daughter board design. Specifying these is outside of the scope of the DNSEAM_NS interface.

### 2.2.3 Signaling Standards for Sideband Signals

This section defines the signaling standards applicable to group 4, “Sideband” signals. The below schematic clipping shows the location of these signals on the DNSEAM_NS motherboard interface header schematic symbol:
Sideband signals shall tolerate a single-ended voltage of between -0.3V to \( V_{CCO} + 0.3V \).

The mother board shall be capable of bi-directional signaling on all group 4 signals. It shall both accept and transmit either LVCMOS or LVDS levels. Nominally, \( V_{CCO} \) will be +1.8V ± 5% and either LVCMOS18 or LVDS levels shall be used. It is highly recommended that daughter boards be designed to accept a \( V_{CCO} \) of between +1.2V ± 5% and +1.8V ± 5% and use LVCMOS12/LVCMOS15 or LVDS levels with these \( V_{CCO} \) voltages. It is also recommended that daughter boards be designed to accept a \( V_{CCO} \) of +2.5V ± 5% and use LVCMOS25 or LVDS levels with this \( V_{CCO} \) voltage.

Since \( V_{CCO} \) is provided by the mother board, the mother board needs only to be compatible with the LVCMOS and LVDS levels associated with the \( V_{CCO} \) voltage it provides.

Single-Ended signaling levels are defined in the following table.

<table>
<thead>
<tr>
<th>Signaling Standard</th>
<th>( V_{IL_MIN} )</th>
<th>( V_{IL_MAX} )</th>
<th>( V_{IH_MIN} )</th>
<th>( V_{IH_MAX} )</th>
<th>( V_{OL_MIN} )</th>
<th>( V_{OL_MAX} )</th>
<th>( V_{OH_MIN} )</th>
<th>( V_{OH_MAX} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVCMOS15</td>
<td>-0.3V</td>
<td>+0.45V</td>
<td>+1.05V</td>
<td>+1.8V</td>
<td>0V</td>
<td>+0.375V</td>
<td>+1.125V</td>
<td>( V_{CCO} )</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>-0.3V</td>
<td>+0.63V</td>
<td>+1.17V</td>
<td>+2.1V</td>
<td>0V</td>
<td>+0.45V</td>
<td>+1.35V</td>
<td>( V_{CCO} )</td>
</tr>
<tr>
<td>LVCMOS25</td>
<td>-0.3V</td>
<td>+0.7V</td>
<td>+1.7V</td>
<td>+2.8V</td>
<td>0V</td>
<td>+0.40V</td>
<td>+2.1V</td>
<td>( V_{CCO} )</td>
</tr>
</tbody>
</table>

LVDS levels are defined in the following table.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Common-Mode</td>
<td>+0.3V</td>
<td>+1.2V</td>
<td>+1.425V</td>
</tr>
</tbody>
</table>

3 Taken from Table 7 of Xilinx DS183, “Virtex-7 Data Sheet”, v1.3 dated February 13, 2012
4 Taken from Table 11 of Xilinx DS183, “Virtex-7 Data Sheet”, v1.3 dated February 13, 2012
<table>
<thead>
<tr>
<th>Input dVpp&lt;sup&gt;5&lt;/sup&gt;</th>
<th>100mV</th>
<th>350mV</th>
<th>600mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Common-Mode</td>
<td>+1.0V</td>
<td>+1.25V</td>
<td>+1.425V</td>
</tr>
<tr>
<td>Output dVpp</td>
<td>245mV</td>
<td>350mV</td>
<td>600mV</td>
</tr>
</tbody>
</table>

LVDS pin pairs are bright yellow pin groups encircled with dotted lines in the below clipping from the pin map. The pin names ending with ‘p’ are the true signal and the pin names ending with ‘n’ are the complementary signal. For LVDS pin pairs, the main board shall ensure that directionality supports that given by the pin map. The daughter board shall be compatible with the directionality of these signals.

The mother board shall implement selectable 100Ω differential termination on all group 4 RX pin pairs.

2.2.3.1 Power-On Sequencing Requirements Related to Group 4 Signals
See section 2.5.3.1.

2.3 Signal Routing Requirements
This section details routing requirements for signal groups 2-4 on the DNSEAM_NS interface.

2.3.1 Routing Requirements for High-Speed Serial Signals
All high-speed serial signals shall be routed as 100Ω differential pairs. Tightly coupled routing is highly recommended. P to N length-matching must be done to within 10 mils.

There shall be no more than 350ps of skew between all group 2 signals on the mother board. There shall be no more than 350ps of skew between all group 2 signals on the daughter board.

The DNSEAM_NS interface specification does not define a maximum signal length for group 2 signals. However, it is highly recommended that trace lengths be kept as short as reasonably possible on both the mother and daughter boards. It is also highly recommended that low-loss dielectrics and extra-wide traces<sup>6</sup> be employed on designs targeting line rates higher than 5Gbps.

---

<sup>5</sup> See Figure 4 for definition of dVpp

<sup>6</sup> Wider than “standard” 4-mil traces.
2.3.2 **Routing Requirements for REFCLK Signals**
All REFCLK signals shall be routed as 100Ω differential pairs. Tightly coupled routing is highly recommended. P to N length-matching must be done to within 10 mils.

The DNSEAM_NS interface specification does not define a maximum signal length for group 3 signals. However, it is highly recommended that trace lengths be kept as short as reasonably possible on both the mother and daughter boards.

2.3.3 **Routing Requirements for Sideband Signals**
All high-speed serial signals shall be routed as 100Ω differential pairs / 50Ω single-ended signals. Loosely coupled routing is highly recommended. P to N length-matching must be done to within 10 mils.

Each of the two sideband signal sub-groups shall be length-matched to 100ps separately on the daughter and mother boards.

2.3.4 **Routing Requirements for Reduced Interfaces**
Groups 2-4 subgroups B shall be unconnected on both mother board and daughter board for reduced pinout interfaces. They shall not have any excess trace length on them.

2.4 **Interface Clocking Requirements**
This section describes the clocking requirements for signal groups 2-4 of the DNSEAM_NS interface.

2.4.1 **High-Speed Serial Clocking**
High-speed serial interfaces typically employ isochronous clocking. An appropriate REFCLK shall be provided for a given line rate, which is mother board transceiver and line rate dependent. The mother board shall accept clocks for HSS-A on either of the REFCLK pairs in RCK-A. The mother board shall accept clocks for HSS-B on either of the REFCLK pairs in RCK-B.

2.4.1.1 **REFCLK Pin Selection Advisory**
It is recommended that if only one REFCLK per Group 3 subgroup is used, that REFCLK_A0 and REFCLK_B0 be used. See section 2.1.2.5.

2.4.1.2 **Bonded Transceiver Clocking Requirements**
A daughter board implementing a HSS protocol requiring four bonded transceivers shall use all transceivers inside one Group 1 subgroup to implement this interface. It will use the corresponding REFCLK (REFCLK_A0 for HSS-A, REFCLK_B0 for HSS-B) to clock this interface. The motherboard will accept the REFCLK and be able to clock the bonded transceivers using it.

A daughter board implementing an HSS protocol requiring eight bonded transceivers will send a REFCLK to both REFCLK_A0 and REFCLK_B0. The motherboard will accept the REFCLK and be able to clock the bonded transceivers using it.

2.4.2 **Sideband Signals Clocking**
Sideband signal clocking will be left up to implementation by the DNSEAM_NS interface. However, there are some requirements for the mother board sideband signal pins.
2.4.2.1 Mother Board Single-Ended Clock Inputs
The mother board shall accept a single-ended clock on pin 83, and be able to use this clock as a synchronous clock for all signals in SB-A. The mother board must also accept a differential clock on 83, 82 for the same purpose.

The mother board shall accept a single-ended clock on pin 78, and be able to use this clock as a synchronous clock for all signals in SB-B. The mother board must also accept a differential clock on 78, 79 for the same purpose.

2.4.2.2 Daughter Board Single-Ended Clock Inputs
If a synchronous interface is to be implemented on signal sub-group SB-A, it is recommended that the daughter board accept either a single-ended clock on pin 81 or a differential clock on pins 81 and 89 and be able to use this clock as a synchronous clock for all signals in SB-A. If single ended clocking is used, it is recommended that the daughter board provide load termination on pin 81. If differential clocking is used, it is required that the daughter board provide 100Ω differential termination across pins 81 and 89.

If a synchronous interface is to be implemented on signal sub-group SB-B, it is recommended that the daughter board accept either a single-ended clock on pin 80 or a differential clock on pins 80 and 72 and be able to use this clock as a synchronous clock for all signals in SB-B. If single ended clocking is used, it is recommended that the daughter board provide load termination on pin 80. If differential clocking is used, it is recommended that the daughter board provide 100Ω differential termination across pins 80 and 72.

2.5 Power Provision
This section details power delivery on the DNSEAM_NS interface. Three power rails are available across the DNSEAM_NS interface header. The below schematic clipping shows the location of group 1 (power) signals on the DNSEAM_NS mother board interface header schematic symbol:

![Schematic Clipping](image)

*Figure 10 - Schematic Clipping Demonstrating Location of Group 1 Signals on DNSEAM_NS Mother Board Header Schematic Symbol*

All three are sourced from the mother board. The rails are +12V, +3.3V, and \( V_{CCO} \). Their nominal voltages and current ratings are described below.
2.5.1  **+12V Rail**
The +12V rail shall be driven by the mother board; it shall provide a voltage of +12V ± 10%. It is intended for use as an input voltage for switching power supplies. The mother board shall provide at least 4A on this rail; the daughter board shall draw no more than 4A.

It is recommended that a 7A or greater fuse be installed in-line on the daughter board for this rail.

2.5.2  **+3.3V Rail**
The +3.3V rail shall be driven by the mother board; it shall provide a voltage of +3.3V ± 5%. It is intended for use as an input voltage for linear drop-out power supplies. The mother board shall provide at least 6A on this rail; the daughter board shall draw no more than 6A.

It is recommended that a 10A or greater fuse be installed in-line on the daughter board for this rail.

2.5.3  **VCCO Rail**
The VCCO rail shall be driven by the mother board; it shall provide a voltage of +1.8V. It is intended for use as a reference voltage for group 4 signals, and as a source voltage for I/O buffers on group 4 signals. The mother board shall provide at least 2A on this rail; the daughter board shall draw no more than 2A.

It is highly recommended that the daughter board tolerate a voltage of between +1.2V and +1.5V on VCCO. It is recommended that the daughter board tolerate a voltage of +2.5V on VCCO.

It is recommended that a 3A or greater fuse be installed in-line on the daughter board for this rail.

2.5.3.1  **Power Sequencing Relative to VCCO**
No signal in group 4 shall be driven above VCCO + 0.3V by either mother board or daughter board. To meet this requirement it is recommended that both mother board and daughter board use VCCO as the VCC rail for their I/O buffers.

2.5.4  **Ground Pins**
There are many ground pins on the DNSEAM_NS interface header. These serve as both as digital ground (i.e. signal return paths and digital power supply grounds) and chassis ground. They shall be connected to digital ground on both mother and daughter boards.
3 Mechanical Requirements

This section will describe the mechanical requirements for the DNSEAM_NS interface. The mechanical requirements include specifying the Samtec SEAM/SEAF connectors used in the interface, describing the board outline, and discussing system-level considerations.

As the DNSEAM_NS Full and Reduced pinouts are mechanically identical, items in this section apply to both the Full and Reduced pinout interfaces.

3.1 Daughter Card Outline Definition

This section will detail the daughter card outlines designated for the DNSEAM_NS interface. Two outline options are provided, full-width and half-width. All daughter boards implementing the DNSEAM_NS interface shall comply with one of these two daughter board outlines. The full-width outline is a full 99mm wide and can host (f.ex.) up to four SFP+ connectors, two Infiniband-CX4 connectors, or two PCI Express Cable connectors. The half-width outline is somewhat narrower in application and can only host (for example) up to two SFP+ connectors. The half-width outline and mounting holes fit completely into those specified for full-width cards. Thus, half-width daughter boards may be used in mother board positions designed for either half-width or full-width daughter boards. Full width daughter boards may only be used in mother board positions designed for full-width mother boards.

In general, it is recommended that main boards make allocation for full-width cards where possible to maximize compatibility with all daughter card form factors.

A daughter card implementing either the full or half-width outline option must cover the entire outline and implement all mounting holes.7 It is recommended that the mother board cover the entire daughter board outline and provide corresponding mounting holes. The mother board shall have matching mounting holes wherever the mother board overlaps a daughter board outline mounting hole.

Exceptions to the requirement to cover the entire outline may be made when an off-board connector placed on the board requires a cut-out or “notch” in the side of the board. In this case the daughter board outline may be resized as appropriate, provided that the connector is placed so as to mate with a chassis aperture plate placed in accordance with section 3.3.1.

3.1.1 Daughter Board Outline, Full-Width

The following diagram describes the DNSEAM_NS full-width daughter board outline. All full-width cards implementing the DNSEAM_NS interface shall comply with this diagram, including all dimensions and mounting hole locations.

---

7 With one exception, see 3.1.1.1
Figure 11 - Illustration of DNSEAM_NS Full-Width Daughter Card Outline

Figure 11 shows the full-width daughter card outline from the component side of the daughter card. The main board shall have the corresponding set of mounting holes to accept either baseplate-mounted standoffs (for chassis applications) or mother board to daughter board standoffs (for non-chassis applications). In this drawing the right edge will be facing the front of the chassis, hence, off-board connectors should be placed along this edge only. Clearance to the inside of the chassis is defined in section 3.3.1.

3.1.1.1 Mounting hole Allowance
For the full outline only, if the mounting hole at co-ordinate (104.75, 55) interferes with HSS connector placement along the right-most edge, this hole can be omitted. It is required that a component and non-ground via/trace keepout for the hole still be enforced on the solder side of the board, since there may be a chassis grounded standoff at this location on the baseplate or mother board.

3.1.2 Daughter Board Outline, Half-Width
The following diagram describes the DNSEAM_NS half-width daughter board outline. All half-width cards implementing the DNSEAM_NS interface shall comply with this diagram, including all dimensions and mounting hole locations.
Proposed Outline (Half-Width)

Figure 12 - Illustration of DNSEAM_NS Half-Width Daughter Card Outline

Figure 12 shows the half-width daughter card outline from the component side of the daughter card. The main board shall have the corresponding set of mounting holes to accept either baseplate-mounted standoffs (for chassis applications) or mother board to daughter board standoffs (for non-chassis applications). In this drawing the right edge will be facing the front of the chassis, hence, off-board connectors should be placed along this edge only.

3.1.3 Note on Main Board Layout for DNSEAM_NS Interface Compatibility
Figure 11 and Figure 12 both illustrate daughter board outlines for the DNSEAM_NS interface. These outline drawings are viewed from the component side of the daughter board, i.e. with the SEAF connector on the back. The mother board outline location and mounting holes should mirror the daughter board outline.

3.1.4 Example Daughter Board Layouts
This section features some example daughter board layouts, in both full-width and half-width outlines. This section does not contain any recommendations or requirements; it exists solely to illustrate how the DNSEAM_NS interface daughter board outlines may be adapter for common use cases.

3.1.4.1 SFP+ 4x Full-Width Card
The below diagram illustrates an example board layout for a full-width daughter board hosting four SFP+ headers.
3.1.4.2 SFP+ 2x, Half-Width Card

The below diagram illustrates an example board layout for a half-width daughter board hosting two SFP+ headers:

**Figure 14 - Example Layout for Half-Width Daughter Board Hosting Two SFP+ Headers**
### 3.1.4.3 SFP+, 8-port Full-Width Card

The below diagram illustrates an example board layout for a full-width daughter board hosting eight SFP+ headers using a four-wide, double-height SFP+ cage.

![SFP 2x4 (Full-Width)](image)

*Figure 15 - Example Layout for Full-Width Daughter Board Hosting Eight SFP+ Cages*
3.1.4.4 PCIe Cable 4-lane, 2x Full-Width Card

The below diagram illustrates an example board layout for a full-width daughter board hosting two PCI Express Cable Headers.

PCI Express Cable, 2x (Full-Width)

Figure 16 - Example Layout for Full-Width Daughter Board Hosting Two PCIe Headers
3.1.4.5 PCIe 8x Full-Width Card
The below diagram illustrates an example board layout for a full-width daughter board a single PCIe 8-lane cable connector.

![Diagram](image_url)

*Figure 17 - Example Layout for Full-Width Daughter Board Hosting One PCIe 8-lane Cable Connector*
3.1.4.6 CX4 2x Full-Width Card
The below diagram illustrates an example board layout for a full-width daughter board hosting two Infiniband CX4 headers:

![Diagram of CX4 2x Full-Width Card]

*Figure 18 - Example Layout for Full-Width Daughter Board Hosting Two Infiniband CX4 Headers*
3.1.4.7  QSFP Half-Width Card
The below diagram illustrates an example layout for a QSFP half-width card.

![QSFP (Half-Width)](image)

Figure 19 - Example Layout for Half-Width Daughter Board Hosting a QSFP Header

3.1.4.8  SMA Full-Width Card
The below diagram illustrates an example board layout for a full-width daughter board hosting lots of SMA coaxial connectors.

![SMAs (Full-Width)](image)

Figure 20 - Example Layout for Full-Width Daughter Board Hosting Many SMA Connectors
3.1.4.9 SATA Full-Width Card

The below diagram illustrates an example board layout for a full-width daughter board hosting four or eight SATA connectors.

![SATA x4 (Full-Width)](image)

*Figure 21 - Example Layout for Full-Width Daughter Board Hosting Four or Eight SATA Connectors*
3.1.4.10 HDMI & DisplayPort Full-Width Card
The below diagram illustrates an example board layout for a full-width daughter board hosting an HDMI port and a DisplayPort connector.

![HDMI & DisplayPort Diagram](image)

*Figure 22 - Example Layout for Full-Width Daughter Board Hosting HDMI and DisplayPort Connectors*

3.2 Mezzanine Stack Description
This section will describe the mezzanine stack. Included will be a specification for the connectors used and drawings for mated connector systems.

3.2.1 Connector Specification
The DNSEAM_NS interface shall use the Samtec SEARAY series of connectors.

- The mother board shall use the **Samtec SEAM-20-07.0-S-08-2-A-K-TR** connector.
  - Dini PID 3356
- The daughter board shall use the **Samtec SEAF-20-05.0-S-08-2-A-K-TR** connector.
  - Dini PID 4139

Each connector shall have a pair of mounting holes, used to secure the connectors together. The holes are to have a 2.8mm diameter drill, and a 5mm diameter keepout.
The position of holes shall comply to that denoted by the following illustrations:

**Detail of SEAM (Main board connector)**

**Outline with Mounting Holes**

(\(\text{origin = connector center}\))

(-14.5, -9)

(-19, 0)

*Note: Connector is mounted on SOLDER SIDE of PCB. This view is therefore looking THROUGH the PCB.*

*Note: Holes to have 2.8mm drill, 5mm keepout, unplated*

**Figure 24 - Illustration of SEAM (mother board) Connector Mounting Holes**
3.2.1.1 Mounting Hole Coverage and Attachment

All mounting holes in each outline shall be used to secure the boards together and possibly to a baseplate, if it is present in the system. If the mother board does not cover the extent of some of the outline and (necessarily) lacks the appropriate mounting holes, provisions shall be made to secure the non-covered mounting holes of the daughter board to a baseplate or similar supporting structure. Consider the following illustration:

In Figure 26, we see that the left-most mounting hole is “covered” by both mother board and daughter board. Here, we attach both mother board and daughter board together to the base plate, using a standoff/screw set. The right-most mounting hole is not covered by the mother board; the mother board’s right-most board edge terminates to the left to this hole. In this case, we use a standoff/spacer/screw set to attach the daughter board directly to the mother board. This application is described in more detail in section 3.2.3.

The daughter board must always fill the entire outline and hence shall implement all mounting holes called out in this specification, with one exception. See section 3.1 for more information about daughter board outlines and mounting hole locations.
3.2.1.2 Connector, Alternate Orientation
For some applications, it may be desirable to place the mother board SEAM connector on the component side of the circuit board. The following connector outline and mounting hole placement should therefore be used:

Detail of SEAM (Main board connector)
Outline with Mounting Holes
Alternate Orientation

Note: Connector is mounted on COMPONENT SIDE of PCB. This view is therefore looking AT the PCB.
Note: Holes to have 2.8mm drill, 5mm keepout, unplated

Figure 27 - Illustration of SEAM (mother board) Connector Mounting Holes, Alternate Orientation

Note that the daughter board connector should always be on the solder side of the daughter board. See sections 3.2.3 and 3.2.4.5 for more information on the Alternate Orientation for daughter board mounting.

3.2.2 Stack Illustration, Baseplate Used (Preferred Orientation)
The DNSEAM_NS interface assumes that that the SEAM and SEAF connectors are both mounted on the “solder side” of the mother and daughter boards respectively. This is termed the “preferred” orientation. Furthermore, the DNSEAM_NS stack for chassis applications assumes a baseplate between the mother and daughter boards. The proposed stack is illustrated below:

Proposed Stack (Chassis, Preferred)

This section will detail the mechanical requirements of the DNSEAM_NS interface with regards to the mezzanine-style stacking orientation when used with a baseplate.

3.2.2.1 Clearance Requirements
The main board shall have backside components (between the main board solder side and chassis baseplate) no taller than 5.35mm. The main board is recommended to have thickness of 0.100”. The
DNSEAM_NS interface makes no recommendations for component side component heights for main boards.

The daughter board shall have backside components (between the daughter board solder side and chassis baseplate) no taller than 4.00mm. The daughter board is recommended to have thickness of 0.062”. All component-side parts on the daughter boards shall be shorter than 27mm for DNSEAM_NS chassis applications.

It is recommended that the top surface of any components taller than 2mm be either electrically insulated or shorted to chassis ground (or equivalent, i.e. digital ground in most applications).

The chassis baseplate is required to have thickness of 0.047”; this corresponds to 18 gauge sheet metal.

### 3.2.2.2 Hardware Requirements, Main Board

It is required that the mainboard be attached to the baseplate using ¼” tall, 3/16” hex outside dimension, 2-56 threaded, male-female standoffs. It is recommended that these standoffs be brass. A drawing of a standoff meeting these requirements is given below:

![CAD Drawing of Example Main Board Standoff for Chassis (Preferred) Applications](image)

It is required that the main board be attached to the standoffs using ¾” long screws, threaded with 2-56 threads. It is recommended that they be allen-head socket cap screws, made of alloy steel, plated with zinc. A drawing of a screw meeting these requirements is given below:
It is required that a washer no thicker than 0.02” be placed between the screw head and the component side of the PCB. A drawing of a washer meeting these requirements is given below.

3.2.2.3 Hardware Requirements, Daughter Board
It is required that the daughter board be attached to the base plate using 3/16” tall, 3/16” male-female 2-56 threaded standoffs. It is recommended that these be brass standoffs. A standoff meeting these requirements is depicted below:
Figure 32 - CAD Drawing of Example Daughter Board Standoff for Chassis (Preferred) Applications

It is required that the daughter board be attached to the standoffs using 3/16” hex nuts with 2-56 threading. It is required that the nut be no taller than 1/16”. A drawing of a nut meeting these requirements is given below:

Figure 33 - CAD Drawing of Example Daughter Board Nut for Chassis (Preferred) Applications

It is required that a washer no thicker than 0.02” be placed between the daughter board nut and the component side of the PCB. A drawing of a washer meeting these requirements is given below.
3.2.2.4 Recommended Hardware Part Numbers
Hardware meeting the requirements of sections 3.2.2.2 and 3.2.2.3 can be ordered from McMaster-Carr. Reference the following part numbers:

Table 3 - Recommended Chassis (Preferred) Mounting Hardware, McMaster-Carr Part Numbers

<table>
<thead>
<tr>
<th>Part Description</th>
<th>McMaster-Carr Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Board Standoff</td>
<td>92700A211</td>
</tr>
<tr>
<td>Main Board Screw</td>
<td>90128A042</td>
</tr>
<tr>
<td>Main Board Washer</td>
<td>90945A705</td>
</tr>
<tr>
<td>Daughter Board Standoff</td>
<td>92700A512</td>
</tr>
<tr>
<td>Daughter Board Nut</td>
<td>96537A110</td>
</tr>
<tr>
<td>Daughter Board Washer</td>
<td>90945A705</td>
</tr>
</tbody>
</table>

3.2.2.5 Mechanical Assembly Illustration
The following is a mechanical assembly illustration for the standoff and board mezzanine stack. This illustration details the stack for chassis and baseplate-mounted applications.
3.2.3 **Stack Illustration, Baseplate Used (Alternate Orientation)**

The DNSEAM_NS allows for the SEAM mother board connector to be mounted on the component side of the mother board. This is termed the “alternate” orientation. The DNSEAM_NS alternate stack for chassis applications assumes a baseplate on the opposite side of the mother board. It is recommended that the mother board cover the entire daughter board outline, so that the two boards may be mated together. If this is not possible, the non-covered daughter board mounting holes must be secured to the baseplate directly.

The proposed stack for this alternate orientation is illustrated below. Note that the right-most daughter board hole in this figure is not covered by the mother board. It attaches to the base plate directly.

![Proposed Stack (Chassis, Alternate)](image)

This section will detail the mechanical requirements of the DNSEAM_NS interface with regards to the mezzanine-style stacking orientation.
### 3.2.3.1 Clearance Requirements

The main board shall have backside components (between the main board solder side and chassis baseplate) no taller than 5.35mm. Within the daughter board outline, the main board shall have topside components no taller than 5.35mm. The main board is recommended to have thickness of 0.100”. The DNSEAM_NS interface makes no recommendations for component side component heights for main boards.

The daughter board shall have backside components (between the daughter board solder side and chassis baseplate) no taller than 4.00mm. The daughter board is recommended to have thickness of 0.062”. All component-side parts on the daughter boards shall be shorter than 27mm for DNSEAM_NS chassis applications.

It is recommended that the top surface of any components taller than 2mm be either electrically insulated or shorted to chassis ground (or equivalent, i.e. digital ground in most applications).

The chassis baseplate is required to have thickness of 0.047”; this corresponds to 18 gauge sheet metal.

### 3.2.3.2 Hardware Requirements, Main Board

It is required that the mainboard be attached to the baseplate using the combination of a ¼” spacer, 15/32” female-female standoff, and 5/8” screw, all threaded for 2-56 threads.

It is recommended that the standoffs be brass. A drawing of a standoff meeting these requirements is given below.

![Fig 37 - CAD Drawing of Example Main Board Standoff for Chassis (Alternate) Applications](image)

Figure 37 - CAD Drawing of Example Main Board Standoff for Chassis (Alternate) Applications
A ¼” threaded standoff with outside diameter of 3/16” tapped for 2-56 thread screws shall be used. It is recommended that the standoff be made of brass. A drawing of a standoff meeting these requirements is given below.

![CAD Drawing of Example Main Board Spacer for Chassis (Alternate) Applications](image)

It is required that the baseplate be attached to the standoffs and spacers using 5/8” long screws, threaded with 2-56 threads. It is recommended that they be allen-head socket cap screws made of alloy steel plated with zinc. A drawing of a screw meeting these requirements is given below:
It is required that a washer no thicker than 0.02” be placed between the screw head and the base plate, and also between the standoff in Figure 37 and the main board PCB. A drawing of a washer meeting these requirements is given below.

![Figure 39 - CAD Drawing of Example Main Board Screw for Chassis (Alternate) Applications](image)

**3.2.3.3 Hardware Requirements, Daughter Board**

It is required that the daughter board be attached to the base plate using ¼” long, 2-56 threaded screws. It is recommended that allen-head socket cap screws, made of alloy steel plated with zinc, be employed. A drawing of a screw meeting these requirements is given below:

![Figure 40 - CAD Drawing of Example Baseplate Washer for Chassis (Alternate) Applications](image)
It is required that a washer no thicker than 0.02” be placed between the screw head and the component side of the PCB. A drawing of a washer meeting these requirements is given below.

**Figure 42 - CAD Drawing of Example Daughter Board Washer for Chassis (Alternate) Applications**

### 3.2.3.4 Recommended Hardware Part Numbers

Hardware meeting the requirements of sections 3.2.2.2 and 3.2.2.3 can be ordered from McMaster-Carr. Reference the following part numbers:

**Table 4 - Recommended Chassis Mounting Hardware, McMaster-Carr Part Numbers**
### Part Description

<table>
<thead>
<tr>
<th>Part Description</th>
<th>McMaster-Carr Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Board Standoff</td>
<td>90308A008</td>
</tr>
<tr>
<td>Main Board Screw</td>
<td>90128A054</td>
</tr>
<tr>
<td>Baseplate Washer</td>
<td>90945A705</td>
</tr>
<tr>
<td>Main Board Standoff (bottom)</td>
<td>90308A103</td>
</tr>
<tr>
<td>Daughter Board Screw</td>
<td>90128A042</td>
</tr>
<tr>
<td>Daughter Board Washer</td>
<td>90945A705</td>
</tr>
</tbody>
</table>

#### 3.2.3.5 Mechanical Assembly Illustration

The following is a mechanical assembly illustration for the standoff and board mezzanine stack. This illustration details the stack for chassis and baseplate-mounted applications.

![Standoff Mechanical Assembly, Chassis Alternate](image)

*Figure 43 - Board Mezzanine Stack Assembly Illustration (Chassis Applications, Alternate)*

#### 3.2.4 Stack Illustration, No Baseplate (Non-Chassis Applications)

The DNSEAM_NS interface assumes that that the SEAM and SEAF connectors are both mounted on the “solder side” of the mother and daughter boards respectively; this is termed the “preferred” orientation. The DNSEAM_NS interface stack assumes no baseplate for chassis-free applications. The proposed stack for chassis-free setups is illustrated below:

![Illustration of Proposed Stack for DNSEAM_NS in Non-Chassis Applications, Preferred Orientation](image)

*Figure 44 - Illustration of Proposed Stack for DNSEAM_NS in Non-Chassis Applications, Preferred Orientation*
This section will detail the mechanical requirements of the DNSEAM_NS interface with regards to the mezzanine-style stacking orientation.

### 3.2.4.1 Clearance Requirements
The main board shall have backside components (between the main board solder side and chassis baseplate) no taller than 5.35mm. The main board is recommended to have thickness of 0.100”. The DNSEAM_NS interface makes no recommendations for component side component heights for main boards.

The daughter board shall have backside components (between the daughter board solder side and chassis baseplate) no taller than 4.00mm. The daughter board is recommended to have thickness of 0.062”. The DNSEAM_NS interface makes no recommendations for component side component heights for daughter boards in non-chassis applications.

It is recommended that the top surface of any components taller than 2mm be either electrically insulated or shorted to digital ground.

### 3.2.4.2 Hardware Requirements
It is required that the mainboard be attached to the daughter board 3/16” hex, 15/32” long female-female 2-56-threaded standoffs. It is recommended that these standoffs be brass. A drawing of a standoff meeting these requirements is given below.

![Figure 45 - CAD Drawing of Example Main Board to Daughter Board Standoff for Non-Chassis Applications](image)

It is required that the main board and the daughter board be attached to the standoffs using ⅜” long screws, threaded with 2-56 threads. It is recommended that they be allen-head socket cap screws made of alloy steel with zinc plating. A drawing of a screw meeting these requirements is given below:
It is required that a washer no thicker than 0.02” be placed between the screw head and the component side of the PCB. A drawing of a washer meeting these requirements is given below.

3.2.4.3 Recommended Hardware Part Numbers
Hardware meeting the requirements of section 3.2.4.2 can be ordered from McMaster-Carr. Reference the following part numbers:
### Table 5 - Recommended Non-Chassis Mounting Hardware, McMaster-Carr Part Numbers

<table>
<thead>
<tr>
<th>Part Description</th>
<th>McMaster-Carr Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board Standoff</td>
<td>90308A008</td>
</tr>
<tr>
<td>Screw</td>
<td>90128A042</td>
</tr>
<tr>
<td>Washer</td>
<td>90945A705</td>
</tr>
</tbody>
</table>

#### 3.2.4.4 Mechanical Assembly Illustration
The following is a mechanical assembly illustration for the standoff and board mezzanine stack. This illustration details the stack for chassis-free applications.

![Standoff Mechanical Assembly, Chassis-Free](image)

*Figure 48 - Board Mezzanine Stack Assembly Illustration (Chassis-free Applications)*

#### 3.2.4.5 Alternate Orientation
The DNSEAM_NS specification provides for an “alternate” orientation of the non-chassis mother-daughter board mounting. Here, the component side of the mother board faces the solder side of the daughter board. The only difference is that the mother board shall have no components taller than 5.35mm within the area of the daughter board outline. Otherwise the same hardware can be used as for the preferred mounting orientation.

![Proposed Stack (Chassis-Free, Alternate)](image)

*Figure 49 - Illustration of Proposed Stack for DNSEAM_NS in Non-Chassis Applications (Alternate Orientation)*

#### 3.3 Chassis and System-Level Requirements for DNSEAM_NS Implementations
This section will describe chassis and system requirements for boards implementing the DNSEAM_NS interface. In particular, the location of the chassis front panel and connector placement guidelines will be described. Power dissipation requirements will also be addressed.
Most of this section may be ignored for chassis-free DNSEAM_NS implementations.

### 3.3.1 Front panel location

The DNSEAM_NS specification assumes that the chassis front panel is located at the east end of the board outlines (see Figure 11, Figure 12). The chassis front panel shall be placed 1mm (nominal) away from the edge of the PCB. The chassis front panel itself shall have thickness 0.036". The opening for connectors shall be 27mm tall and extend along the east edge of the DNSEAM_NS daughter card outline, to within 6mm of the north and south ends of the edge.

Any connector placement on a DNSEAM_NS daughter board shall tolerance a front plate placement tolerance of +1mm, -0.5mm from the nominal measurements given in the previous paragraph. The below drawing depicts the placement of the front panel relative to the daughter board PCB.

**Figure 50 - Daughter Board Front Panel Opening, Side View**

**Figure 51 - Daughter Board Front Panel Opening, Top View**
3.3.2 **Front panel connector opening**

The front panel connector opening, termed the header aperture, shall be centered on the DNSEAM_NS daughter board east edge. For full-width daughter board outlines, it shall be 87mm wide. For half-width daughter board outlines, it shall be 35mm wide. The below drawings depict the header aperture plate, including the connector opening dimensions.

![Front View, Header Aperture Plate, Full-Width](image)

*Figure 52 - Header Aperture Plate, Including Front-Panel Opening (Front View)*

![Top View, Header Aperture Plate, Full-Width](image)

*Figure 53 - Header Aperture Plate (Top View)*

The header aperture plate shall attach to the main chassis front plate with four ¼” 2-56 screws, as in the above drawings. See Figure 30 for an illustration of a screw meeting these requirements. A washer shall also be employed, see Figure 31 for a washer that meets these requirements.

3.3.3 **Daughter Board Component Height Limitation**

In section 3.2 we define a daughter card solder side component height limitations. The daughter board component side height limit shall be 28mm. It is recommended that any components taller than 20mm have their tops be either insulated or shorted to digital ground.
3.3.4 **Power Dissipation**

The system design shall make provision for the daughter card to dissipate the maximum rated power that the DNSEAM_NS interface provides via the Group 4 Power pins (section 2.5). Any additional power dissipation on the card, made possible (for example) through an external power header, is not accounted for by the system-level provisions of the DNSEAM_NS specification.

The chassis shall provide an ambient air temperature of no warmer than 50°C. There is no minimum chassis airflow guaranteed for the DNSEAM_NS daughter board.