Features

- **DINAR1** daughter card
  - Standalone operation supported with external power supply and loopback card
- Dual HDMI receiver channels (v1.4a) using ADV7612
  - HDTV formats up to 1080p 36-bit Deep Color
  - Display resolutions up to UXGA (1600 × 1200 at 60 Hz)
- Single HDMI output (v1.4) using ADV7511
  - DVI 1.0-compatible transmitter
  - All HDTV formats including 1080p with 12-bit Deep Color
  - Audio return channel (ARC)
  - 3D video.
- Xilinx Kintex-7 FPGA (FFG676), primary for voltage translation:
  - 7K410T-3,-2,-1, 7K325T-3,-2,-1, 7K160T-3,-2,-1 (fastest to slowest)
  - ~3 million ASIC gates (ASIC measure) when stuffed with 7K410T
  - 254k flip-flop/6-input LUTs (708k total FFs)
  - 3.578 Kbytes total FPGA block memory (1590, 18-kbit blocks)
  - 1540, 25x18 multipliers

Table 1: Kintex-7

<table>
<thead>
<tr>
<th>Kintex-7 FPGA</th>
<th>Speed Grades (slowest to fastest)</th>
<th>LUT Size</th>
<th>FF's</th>
<th>Gate Estimate</th>
<th>Max I/O's</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>6-input</td>
<td></td>
<td>Max (100% util) (1000's)</td>
<td>Practical (60% util) (1000's)</td>
<td>Multipliers (25x18)</td>
</tr>
<tr>
<td>7K410T</td>
<td>-1,-2,-3</td>
<td>508,400</td>
<td>4,881</td>
<td>2,930</td>
<td>500</td>
<td>1,540</td>
</tr>
<tr>
<td>7K325T</td>
<td>-1,-2,-3</td>
<td>407,600</td>
<td>3,913</td>
<td>2,350</td>
<td>500</td>
<td>840</td>
</tr>
<tr>
<td>7K160T</td>
<td>-1,-2,-3</td>
<td>202,800</td>
<td>1,947</td>
<td>1,170</td>
<td>400</td>
<td>600</td>
</tr>
</tbody>
</table>

Block Diagrams
Description

Overview
The DINAR1_HDMI_ETH_USB is a daughter card that adds HDMI receive and transmit interfaces to the DINI Group line of FPGA-based ASIC prototyping products. This card can be used standalone. Standalone operation requires loopback board on the DINAR1 connector (provided) and a separate ATX power supply.

HDMI – Receive and Transmit
The DINAR1_HDMI_ETH_USB has two HDMI receive channels and a single HDMI transmit channel. The Analog Devices ADV7511 is used for the transmit channel. This transmitter features full version 1.4 compliance including Audio return channel (ARC) and 3D video support. All features of the chip are available including DVI. A list of the functionality contained in the ADV7511 is best gotten from the datasheet here: ADV7511 Datasheet.

The Analog Devices ADV7612 is used for the receive channels. This chip supports dual HDMI channels and is fully v1.4a compliant. As with the ADV7612, it is best to get the full list of functionality from the datasheet: ADV7612 Datasheet.

The FPGA – Xilinx Kintex-7
We use a single FPGA from the Xilinx Kintex-7 in the FFG676 package, primarily for voltage translation. This package has 400 I/O with the majority utilized.

Three possible FPGAs can be stuffed: 7K410T, 7K325T, and 7K160T. All three FPGAs come in a variety of speed grades (-1,-2/2L, -3) with -3 being the fastest. All speed grades are applicable to this application. Table 1 depicts the resources of the FPGAs with the extreme Xilinx marketing exaggerations remorselessly severed. These are large but low-cost FPGAs. The 7K410T is capable of handling ~3M ASIC gates of logic, with the 7K325T capable of ~2.3 million gates. Features of the Kintex-7 FPGAs include efficient, dual-register 6-input look-up table (LUT) logic, 18 Kb (2 x 9 Kb) block RAMs, and second generation DSP48E1 slices (includes 25 x 18 multipliers). Floating point functions can be implemented using these DSP slices. 100% of the FPGA resources are available for your use. This FPGA is vast overkill for voltage translation.
### DDR3 DRAM - A large amount of local, bulk memory

A single PC3-10600 DDR3 memory in a 256M x 16 configuration is provided on a high performance I/O bank. This DDR3 memory is intended for HDMI frame buffering, but can be used for any purpose. The Xilinx Memory Interface Generator (MIG) is used to provide the memory controller. As always, we supply examples and reference designs to help you with all of your memory interface issues. Please check with us to make sure that what we ship for no charge meets your requirements.

### Miscellaneous Peripherals

Dual RS232 ports, a 1000-baseT Ethernet Phy, and a USB3.0 interface are provided. Also, a standard ARM JTAG interface connector enables ARM debug if you put one of those processors in the FPGA.

### DINAR1 Connector

The DINAR1_HDMI_ETH_USB uses a connector standard called DINIARRAY (DINAR1), which utilizes 320-pin Samtec SEAM series connectors. This board is intended to mate to any DINI Group ASIC Prototyping card with a DINAR1 interface. Where applicable, the signals are routed differentially and can run at the limit of the Virtex-7/Kintex-7 FPGA I/Os: 710 MHz (assumes -2 or faster).

### Status LEDs, Debug

As with all of our ASIC emulation boards, the DINAR1_HDMI_ETH_USB is loaded with LEDs. The LEDs can be used to test mood lighting around your HDMI monitor. When testing this make sure an adult is present and don’t fall asleep. These LEDs are user controllable from the FPGAs so can be used as visual feedback in addition the somnolence enhancement. A JTAG connector provides an interface to ChipScope and other third party debug tools.

### Photos

![Photos](image-url)