The *DINI* Group

DN2000k10
PCI Hosted, ASIC Prototyping Engine

### Features

- Configurations starting at $4,950
- 32/64 bit PCI-based PWB with one to six interconnected Virtex™ FPGAs (BGA560)
- 300k-2 million ASIC gates per PWB
- Stackable to 4 (or more) PWB's
- Flexible, abundant and configurable embedded memory:
  - up to 16 kbytes dual port RAM per FPGA
  - plus up to 49 kbytes per FPGA LUT configured RAM
- HW locking mechanisms for IP protection
- 4 low skew clocks:
  - PCI Clock
  - 2 socketed oscillators
  - 1 user configurable via CPLD
- Fast 32/64 bit PCI host for configuration and test
- Robust observation/debug with 450 connections for logic analyzer observability or for pattern generator stimulus
- Status LED's
- User designed daughter PWB for custom circuitry

### Description

The DN2000k10 is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN2000k10 can be hosted in 32/64 bit PCI slot, or can be used stand-alone. A single DN2000k10 with all six FPGA's stuffed can emulate up to 2 million gates of logic as measured by LSI. Multiple DN2000k10's can be stacked to get even more total logic gates.

The DN2000k10 achieves high gate density and allows for fast target clock frequencies by utilizing one, four, or six FPGAs from Xilinx's Virtex™ family for logic and memory. High I/O-count BGA packages are employed allowing for abundant, fixed interconnect between FPGA's. 450 test pins are provided on both the top and bottom of the PWB for the purpose of stacking up to four PWB's to increase the amount of logic, for logic analyzer-based debugging, or for pattern generator stimulus. Custom daughter cards can be mounted to these pins to interface the DN2000k10 to application specific circuits. A Verilog and VHDL reference PCI target design and test bench is provided at no additional cost. PWB configurations can be stored in the FLASH, and jumpers are provided to switch between configurations. Eight
LED’s are connected to the CPLD and each LED can be user-configured to provide valuable visual feedback.

**Global Clocks**

Four global clocks are provided. Two clocks are from socketed oscillators which can be stuffed by the user. An eight pin, 0.3”, half size DIP package is used and dozens of frequencies are readily available from components suppliers. The third clock is from the CPLD and is user configurable. A fourth clock is the PCI clock from the PCI connector. Special low skew buffers and careful trace routing assure clock integrity on the PWB and across multiple, stacked PWB’s. See figure 3 for clock structure details. Additional clocks may be brought via any of the test connectors for a total of eight. Note that additional clocks can be routed using the MB bus since this bus connects to all six of the FPGA’s. Clocks are not routed through any programmable structures so no skewing exist.

**IP Protection**

HW-based security mechanisms can be employed using a FLASH-based CPLD with the security fuse programmed, effectively protecting the IP and bit streams from hostile parties. Approximately 40 flip-flops are available in the CPLD after configuration issues for this or any other function the user sees fit. Interlocking circuits such as a non-linear feedback shift registers or encrypted ID’s can be placed in the CPLD and handshaking mechanisms with the FPGA’s can be added. A CPLD fashioned in this manner with the
security fuse blown effectively prevents unscrupulous parties from gaining access to the valuable intellectual property.