**Features**

- 32/64-bit, +3.3V, PCI/PCIX-based PWB
- Single Stratix FPGA in BGA1508
  - EP1S40, 1S60, 1S80
- Four external 512k x 36 SSRAM’s
- One 72-bit SDRAM DIMM
  - Enough addressing for up to 1 GB x 72 (8 GB!)
  - Shipped standard with a 512MB SDRAM DIMM PC 133
- One 72-bit DDR SDRAM DIMM
  - Enough addressing for up to 1 GB x 72 (8 GB!)
  - Shipped standard with a 512MB DDR SDRAM
- Two 200-pin high-speed connectors for awesome signal integrity
- 5A onboard linear regulator for +1.5V
- 5A onboard switching regulator for +2.5V and +1.5V
- 10A switching regulator for +3.3V
- Standalone operation via separate power connector
  - +3.3V not needed on backplane
- Fast/Easy FPGA configuration via standard SmartMedia FLASH card
  - Microprocessor controlled
  - RS232 port for configuration/operational status and control
  - Fastest possible configuration using parallel data path
  - Sanity checking programs for bit files eases configuration hassles
- 242 signals for observation/debug
  - Fully compatible with the DN3k10SD
- 6 low skew clocks distributed to FPGA’s and test connector:
  - 2 CY7B994 RoboClockII PLL’s for the best clock distribution
  - 1 FCT3805 low-skew clock driver (non-PLL)
  - 2 user-selectable socketed oscillators
  - PCI/PCI-X clock
- -1 dividable clock via CPLD
- Boatloads of reference stuff included (FREE)
  - 32-bit target PCI design (Verilog/VHDL)
  - 32-bit master/target OpenCore PCI (Verilog)
  - SDRAM controller (Verilog/VHDL)
  - SDRAM controller
  - SOS-based utilities
  - Board test
  - PCI Drivers (with C code)
    - Windows XP, ME, 2000, 98, NT
    - LINUX
    - Solaris
- Full support for embedded logic analyzers
  - SignalTap
  - Identify™ (Bridges2Silicon)

**Description**

The DN5000K10S is a complete logic emulation system that enables ASIC or IP designers to prototype logic and memory designs for a fraction of the cost of other solutions. The DN5000K10S can be hosted in 32/64-bit PCI/PCIX slot, or can be used standalone. A DN5000K10S can emulate up to 600,000 gates of logic as measured by LSI. The DN5000K10S achieves high gate density and allows for fast target clock frequencies by utilizing Altera’s Stratix family of FPGA’s for logic and memory. A high I/O count, 1508-pin BGA package is employed allowing for a host of features including test signals and external memory. A total of 242 signals are provided on the top of the PWB for logic analyzer-based debugging, or for pattern generator stimulus. Custom daughter cards can be mounted to these connectors as a means of interfacing the DN5000K10S to application-specific circuits. A reference 32-bit PCI target design and test bench is provided (in Verilog/VHDL) at no additional cost.
Easy Configuration Via SmartMedia

The configuration bit files for the FPGAs are copied onto a 16/32/64/128-megabyte SmartMedia FLASH card (provided) and an on-board microprocessor controls the FPGA configuration process. An RS232 port provides detailed information regarding the configuration process, completely bypassing time-consuming debugging of the configuration process. Eight LED’s provide instant status and operational feedback. Four of these LED’s are connected to the CPLD and can be user-configured.

Included Accessories

For technical applications and sales support, call 858.454.3419