**Features**

- **USB-based hosted logic prototyping system**
  - Available with up to 9 VirtexII-Pro FPGA's (FF1704 BGA)
    - 2vp70-5,-6,-7 or 2vp100-5,-6
    - 12 DDR SDRAM's (standard: 32M x 16)
  - Options for 64 x 16 DDR devices
  - 2 DDR's connected to FPGA's A, C, D, F, G, I
  - Five 64 Mbit (4M x 16) FLASH devices for PowerPC code storage or other use apps.
  - Connected to FPGA's A, B, C, G, I
  - Large, high-speed busses between FPGA's facilitate the logic partitioning process
  - RocketI/O connections between FPGA's enables high speed data movement
- Two PowerPC 405 Cores per FPGA (18 total with nine FPGA's)
  - Embedded 300+ MHz Harvard Architecture
  - Hardware Multiply/Divide Unit
  - Thirty-Two 32-bit General Purpose Registers
  - 16 KB 2-Way Set-Assoc. Instruction Cache
  - 16 KB 2-Way Set-Assoc. Data Cache
  - Memory Management Unit (MMU)
  - Timer Facilities
- **Dedicated external JTAG connectors for uP trace/debug on FPGA's A & C**
- Six RS232 ports for PowerPC observation/debug
  - Four full duplex (RX/TX)
  - Two Single duplex (TX only)
- **All six ports multiplexed via SpartanII Configuration FPGA**
- **Flexible, abundant, and configurable embedded memory in FPGA's**
  - 444 18-kbit memory blocks per FPGA
  - 2VP100
  - Up to 1.378 Kbytes Distributed SelectRAM per FPGA (2VP100)
  - 100% available for user applications
- **Support for Synplicity's Certify (a partitioning tool)**
  - Direct support for TDM interconnect multiplexing
  - Certify partitioning files provided
- **20A on-board switching regulator for both +3.3V and +1.5V**
- **Status LED's provide instant status and operational feedback**
- **Fast/Easy FPGA configuration via standard SmartMedia FLASH card**
  - Microprocessor controlled (CY7C68013)
  - Separate RS232 port for configuration / operational status and control
  - Fastest possible configuration using SelectMap
  - Nine 2VP100's configures in less than 7 seconds
  - Sanity checking programs for bit files simplify the configuration process
- **5 low skew clocks distributed to all FPGA's and headers (from up to 8 possible sources):**
  - 2 socketed oscillators
  - 1 clock dividable via CPLD
  - 4 external clocks via ribbon cable (may be differential)
  - 2 CY7B993/4 RoboClockII PLL's
- Robust observation/debug with 480+ connections for logic analyzer observability and pattern generator stimulus. Fully compatible with:
  - DNPMC104 -- Embedded Systems Board Carrier (ESBC)
    - PMC and PC/104+ cards
    - DN3k10SD – Observation Daughter Card
    - DN3k10SD_MICTOR – Observation Daughter card with Mictor connectors
- **Custom daughter PWB for application specific circuitry and interfaces**
- **8 off-board, RocketI/O-based high speed serial ports**
  - SMB Connectors (2 MGT’s each)
  - 2 ports each connected to FPGA's A, C, G, I
- **Boatloads of reference stuff included (FREE)**
  - DDR SDRAM controller (Verilog/VHDL)
  - PowerPC ‘Hello World’
  - UART’s
  - USB utilities
  - Board test(s)
  - USB Drivers (with C code)
    - Windows XP, ME, 2000, 98, NT
    - LINUX, Solaris
- **Full support for embedded logic analyzers via JTAG interface**
  - ChipScope, ChipScope PRO
  - Identify™ from Synplicity

**Description**

The DN6000k10 is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN6000k10 is stand-alone or hosted via a USB interface. A single DN6000k10 configured with nine 2VP100's can emulate up to 6 million gates of logic as measured by LSI. And this number does not include the embedded memories and multipliers resident in each FPGA. The DN6000k10 achieves high gate density and allows for fast target clock frequencies by utilizing FPGA's from Xilinx's VirtexII-Pro family for logic and memory. High I/O-count, 1704-pin, flip-chip BGA packages are employed providing for abundant, fixed interconnect between the FPGA's. RocketI/O's are connected between FPGA's, enabling data transfer between FPGA's on the order of gigabytes per second. A total of 480+ test pins are provided on the top of the PWB for logic analyzer-based debugging, or for pattern generator stimulus. The DNP PMC104 card can be mounted to any of these connectors, enabling an interface to A/D’s, D/A’s, and a host of other embedded system peripherals. Also, custom daughter cards can be mounted to these connectors as a means to interface the DN6000k10 to application-specific circuits. Eight RocketI/O ports are reserved for high-speed serial off-board interfaces. Reference material such as DDR SDRAM controllers, flash controllers, and PowerPC code is included (in Verilog, VHDL, C) at no additional cost.
Easy Configuration Via SmartMedia

The configuration bit files for the FPGA's are copied onto a 32/64/128-megabyte SmartMedia FLASH card (provided) and an on-board Cypress microprocessor controls the FPGA configuration process. FPGA configuration can also be controlled via the USB interface. Visibility into the configuration process is enhanced with an RS232 port. Sanity checks are performed automatically on the configuration bit files, streamlining the configuration process. FPGA configuration occurs at the fastest possible SelectMap frequency - 48MHz. Multiple LED's provide instant status and operational feedback.
Included Accessories

- Datasheet:  
  http://www.dinigroup.com/products/6000k10.html

- Users' Manual:  