Product Brief
February 2004
Ver. 1.4

VirtexII™-Pro Based ASIC Prototyping Engine

Features

- 32/64-bit, +3.3V, PCI/PCIX-based PWB
- Single VirtexII-Pro FPGA in FF1152
- Two external independent SSRAM's
- -16M x 16
- One independent external FLASH memory
- 8 High Speed serial ports
- -4 SMA (2 MGT’s)
- One 200-pin high-speed connector for
- -observation daughter cards (such as
- -custom daughter cards
- observation daughter cards)
- -4 SMA (2 MGT’s)
- Two independent DDR SDRAM's
- -2vp20, 2vp30, 2vp40, or 2vp50
- Two external independent SSRAM's
- -2vp20, 2vp30, 2vp40, or 2vp50
- One 200-pin high-speed connector for
- up trace/debug
- RS232 ports for PowerPC processor visibility
- -2 Tx/Rx, 2 Tx only
- Standalone operation via separate power
- -+3.3V not needed on backplane
- Fast/Easy FPGA configuration via standard
- SmartMedia FLASH card
- Microprocessor controlled (Atmega128L)
- -RS232 port for configuration/operational
- status and control
- -Fastest possible configuration using
- SelectMap parallel
- -2vp50 configures in 1 second
- -Sanity checking programs for bit files eases
- configuration hassle

- Two PowerPC 405 Cores
- -Embedded 300+ MHz Harvard Architecture
- Hardware Multiply/Divide Unit
- -Thirty-Two 32-bit General Purpose Registers
- -16 KB 2-Way Set-Associative Instruction Cache
- -16 KB 2-Way Set-Associative Data Cache
- -Memory Management Unit (MMU)
- -Timer Facilities
- -One dedicated external JTAG connectors for
- -up trace/debug
- 6 low skew clocks distributed to FPGA’s and test
- connector:
- -2 CY7B994 RoboClockII PLL’s for the best
- clock distribution
- -2 user-selectable socketed oscillators
- -PCI/PCI-X clock
- -1 dividable clock via CPLD
- Boatloads of reference stuff included (FREE)
- -32-bit target PCI design (Verilog/VHDL)
- -32-bit master/target OpenCore PCI (Verilog)
- -SDRAM controller (Verilog/VHDL)
- -DDR SDRAM controller (Verilog/VHDL)
- -PowerPC ‘Hello World’
- -UARTs
- -DOS-based utilities
- -Board test(s)
- -PCI Drivers (with C code)
- Windows XP, ME, 2000, 98, NT
- LINUX, Solaris
- Full support for embedded logic analyzers
- -ChipScope, ChipScope PRO
- -Identify™ from Synplicity

The
DiNi
Group
Description

The DN6000k10SC is a complete logic emulation system that enables ASIC or IP designers to prototype logic, memory, and embedded systems designs for a fraction of the cost of other solutions. The DN6000k10SC can be hosted in 32/64-bit PCI/PCIX slot, or can be used standalone. A DN6000k10SC can emulate up to 350,000 gates of logic as measured by LSI. In addition, the VirtexII Pro FPGA contains two 300MHz+ 405 PowerPC microprocessors, 88-232 18x18 multipliers, and more than 438 Kbytes of block RAM memory. Eight serial RocketI/O ports are provided on the top of the circuit board and can support a variety of serial communication protocols at speeds up to 3.125 GB/s, with 10 GB/s to follow. The DN6000k10SC is designed for performance and low cost – all external memories run at a frequency of at least 133MHz and the FPGA internal speed is limited only by the logic within. A high I/O count, 1152-pin BGA package is employed allowing for a host of external interface features including test signals, two SSRAM’s, two DDR SDRAM’s, and one FLASH. A total of 162 signals are provided via a 200-pin connector on the top of the PWB for logic analyzer-based debugging, or for pattern generator stimulus. Custom daughter cards can be mounted to this connector to interface the DN6000k10SC to application-specific circuits. A reference 32-bit PCI target design and test bench is provided (in Verilog/VHDL) at no additional cost.

Easy Configuration Via SmartMedia

The configuration bit file for the FPGA is copied onto a 32/64/128-megabyte SmartMedia FLASH card (provided) and an on-board microprocessor controls the FPGA configuration process. An RS232 port provides detailed information regarding the configuration process, completely bypassing time-consuming debugging of the configuration process. FPGA configuration occurs at close to the fastest possible parallel frequency --48MHz. Eight LED’s provide instant status and operational feedback. Two of these LED’s are connected to the CPLD and can be user-configured.

Included Accessories

<table>
<thead>
<tr>
<th>DN6000K10SC STUFFING OPTIONS</th>
<th>ZP50</th>
<th>ZP30</th>
<th>ZP20</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSRAM’s</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>DDR’s</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>FLASH</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SMA</td>
<td>4</td>
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<td>4</td>
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</table>

For technical applications and sales support, call 858.454.3419

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