Features

- 32/64-bit, +3.3V, PCI/PCI-X-based PWB
- Single Virtex-II Pro FPGA in FF1704
- -2vp70-5,-6,-7, 2vp100-5,-6, 2vp70-5,-6,-7
- Four external independent SSRAM’s - 512kb x 36 (pipeline)
- Options to 1M & ZBT, flowthrough
- Four independent DDR SDRAM’s
- -162 signals for observation/debug
  - 2 SATA (2 MGT’s)
  - 1 GigE Fiber (4 MGT’s) (optional)
- 10 High Speed serial ports
  - 1 GigE Fiber (4 MGT’s) (optional)
  - 2 HSSDC2 - Infiniband (2 MGT’s)
  - 2 SATA (2 MGT’s)
  - 2 SMA (2 MGT’s)
- One 200-pin high-speed connector for awesome signal integrity
  - custom daughter cards
  - observation daughter cards (such as DN3k10SD)
- 162 signals for observation/debug
  - Fully compatible with the DN3k10SD
- 5A onboard linear regulator for +1.5V
  - +1.5V @ 10A Switcher Module
  - +2.5V @ 10A Switcher Module
  - +3.3V @ 10A Switcher Module
- Two PowerPC 405 Cores
  - Embedded 300+ MHz Harvard Architecture
  - Hardware Multiply/Divide Unit
  - Thirty-Two 32-bit General Purpose Registers
  - 16 KB 2-Way Set-Associative Instruction Cache
  - 16 KB 2-Way Set-Associative Data Cache
  - Memory Management Unit (MMU)
  - Timer Facilities
  - One dedicated external JTAG connectors for uP trace/debug
- RS232 ports for PowerPC processor visibility
  - -2 Tx/Rx, 2 Tx only
- Standalone operation via separate power connector
  - +3.3V not needed on backplane
- Fast/Easy FPGA configuration via standard SmartMedia FLASH card
  - Microprocessor controlled (Atmega128L)
  - RS232 port for configuration/operational status and control
  - Fastest possible configuration using SelectMap parallel
  - -2vp70 configures in 1 second
  - Sanity checking programs for bit files eases configuration hassles
- 6 low skew clocks distributed to FPGA’s and test connector:
  - -2 CY7B994 RoboClock II PLL’s for the best clock distribution
  - -1 FCT3805 low-skew clock driver (non-PLL)
  - -2 user-selectable socketed oscillators
  - -PCI/PCI-X clock
  - -1 dividable clock via CPLD
- Bootloads of reference stuff included (FREE)
  - -32-bit target PCI design (Verilog/VHDL)
  - -32-bit master/target OpenCore PCI (Verilog)
  - -SDRAM controller (Verilog/VHDL)
  - -DDR SDRAM controller (Verilog/VHDL)
  - -PowerPC ‘Hello World’
  - -UARTs
  - -DOS-based utilities
  - -Board test(s)
  - -PCI Drivers (with C code)
  - Windows XP, ME, 2000, 98, NT
  - -LINUX, Solaris
- Full support for embedded logic analyzers
  - -ChipScope, ChipScope PRO
  - -Identify™ from Synplicity
Description

The DN6000K10S is a complete logic emulation system that enables ASIC or IP designers to prototype logic, memory, and embedded systems designs for a fraction of the cost of other solutions. The DN6000K10S can be hosted in 32/64-bit PCI/PCIX slot, or can be used standalone. A DN6000K10S can emulate up to 600,000 gates of logic as measured by LSI. In addition, the VirtexII Pro FPGA contains two 300MHz+ PowerPC microprocessors, 328-556 18x18 multipliers, and more than 438 Kbytes of block RAM memory. Ten serial RocketI/O ports are provided on the top of the circuit board and can support a variety of serial communication protocols at speeds up to 3.125 GB/s (requires -6 or -7 speed grade), with 10 GB/s to follow. The DN6000K10S is designed for performance – all external memories run at a frequency of at least 133MHz and the FPGA internal speed is limited only by the logic within. A high I/O count, 1704-pin BGA package is employed allowing for a host of external interface features including test signals, four SSRAM’s, four DDR SDRAM’s, and two FLASH’s. A total of 162 signals are provided via a 200-pin connector on the top of the PWB for logic analyzer-based debugging, or for pattern generator stimulus. Custom daughter cards can be mounted to this connector to interface the DN6000K10S to application-specific circuits. A reference 32-bit PCI target design and test bench is provided (in Verilog/VHDL) at no additional cost.

Easy Configuration Via SmartMedia

The configuration bit file for the FPGA is copied onto a 32/64/128-megabyte SmartMedia FLASH card (provided) and an on-board microprocessor controls the FPGA configuration process. An RS232 port provides detailed information regarding the configuration process, completely bypassing time-consuming debugging of the configuration process. FPGA configuration occurs at close to the fastest possible parallel frequency --48MHz. Eight LED’s provide instant status and operational feedback. Two of these LED’s are connected to the CPLD and can be user-configured.

Included Accessories

For technical applications and sales support, call 858.454.3419