VirtexII™-Pro Based ASIC Prototyping Engine (PCIe)

Features

- PCI Express (PCIe) PWB (8-lane or 1-lane)
- Single VirtexII-Pro or Pro X FPGA in FF1704
- 10 high speed serial ports
  - 2 GbE FIBER (SFP) (optional)
  - 2 HSSDC2 — Infiniband (2 MGTs)
  - 4 SMA (4 MGTs)
  - 2 SATA (2 MGTs)
- One 200-pin high-speed expansion connector for awesome signal integrity
  - custom daughter cards
  - observation daughter cards (such as DN3k10SD)
- 161 signals for observation/debug
- Four independent DDR SDRAMs
- 32Mx16 (256MB Total) with options to 64Mx16 (512MB Total)
- Two independent external FLASH memories
- 4Mx16
- Four external independent SSRAMs
- 512k x 36 (pipeline)
- Options to 1M/2M & ZBT (NoBL)
- Onboard Power Supplies
  - +1.5V@ 10 A switcher module
  - +2.5V@ 10 A switcher module
- Two PowerPC 405 Cores
  - Embedded 300+ MHz Harvard Architecture
  - Hardware Multiply/Divide Unit
  - Thirty-two 32-bit General Purpose Registers
  - 16 kb 2-Way Set Assoc. Instruction Cache
  - 16 kb 2-Way Set Assoc. Data Cache
  - Memory Management Unit (MMU)
  - Timer facilities
  - One dedicated external JTAG connector for µP trace/debug
- RS232 ports for PowerPC processor visibility
  - 1 Tx/Rx, 2 Tx only
- Standalone operation via separate power connector
  - +3.3 V not needed on backplane
- Fast/Easy FPGA configuration via standard SmartMedia FLASH card
  - Microprocessor controlled (AtMega128L)
- Fast/Easy FPGA configuration via standard
  - SmartMedia FLASH card
  - RS232 port for configuration/operational status and control
  - Fastest possible configuration using SelectMap parallel
- 2vp70 configures in 1 second
- Sanity checking programs for bit files eases configuration hassles
- 6 low skew clocks distributed to FPGAs and test connector:
  - 2 CY7B994 RoboClockII PLLs for the best clock distribution
  - 1 FCT3805 low-skew clock divider (non-PLL)
  - 2 user-selectable socketed oscillators
  - PCI/PCI-X clock
  - 1 dividable clock via CPLD
- Boatloads of reference stuff included FREE
  - SDRAM controller (Verilog/VHDL)
  - DDR SDRAM controller (Verilog/VHDL)
  - PowerPC “Hello, World”
  - UARTs
  - DOS-based utilities
  - Board test(s)
  - PCI Drivers (with C code)
  - Windows XP, ME, 2000, 98, NT
  - LINUX, Solaris
- Full support for embedded logic analyzers
  - ChipScope, ChipScope PRO
  - Identify™ from Synplicity

The DINI Group
Description

The DN6000k10SE is a complete FPGA-based logic emulation system that enables ASIC or IP designers to prototype PCI Express (PCIe) logic, memory, and embedded systems designs for a fraction of the cost of other solutions. The DN6000k10SE is available in 1-lane and 8-lane version, and can be used standalone if necessary. A DN6000k10SE can emulate up to 600,000 gates of logic as measured by LSI. In addition, the VirtexII Pro FPGA contains two 300MHz+ 405 PowerPC microprocessors, 328-556 18x18 multipliers, and more than 438 Kbytes of block RAM memory. Ten serial Rocket I/O ports are provided on the top of the circuit board and can support a variety of serial communication protocols at speeds up to 3.125GB/sec (requires -6 or -7 speed grade.) A -6 speed grade part (or faster) is necessary to support the Xilinx PCI Express IP. The DN6000k10SE is designed for performance— all external memories run at a frequency of at least 133 MHz and the internal speed of the FPGA is limited only by your logic. A high I/O count, 1704-pin BGA package is employed, allowing for a host of external interface features including test signals, four SSRAMs, four DDR SSRAMs, and two FLASHs. A total of 161 signals are provided via a 200-pin connector on the top of the PWB for logic analyzer-based debugging, or for pattern generator stimulus. Custom daughter cards can be mounted to this connector to interface with the DN6000K10SE to application-specific circuits.

Easy Configuration Via SmartMedia

The configuration bit file for the FPGA is copied onto a 32/64/128-megabyte SmartMedia FLASH card (provided) and an on-board microprocessor controls the FPGA configuration process. An RS232 port provides detailed information regarding the configuration process, completely bypassing time-consuming debugging of the configuration process. FPGA configuration occurs at close to the fastest-possible parallel frequency—48 MHz. Eight LEDs provide instant status and operational feedback. Two of these LEDs are connected to the CPLD and can be user-configured.

Included Accessories:

For technical applications and sales support, call 858.454.3419