Features

- PCI hosted logic prototyping system available with up to 3 Altera StratixII FPGA's (1508 BGA):  
  - EP2S90-5, -4, -3  
  - EP2S130-5, -4, -3  
  - EP2S180-5, -4, -3  
  - 100% FPGA resources available for user application  
  - Nearly 3.7M ASIC gates (LSI measure)  
- FPGA to FPGA interconnect LVDS differential - 500Mhz differential FPGA to FPGA - Reference designs for integrated I/O SERDES - 10x pin multiplexing per LVDS pair with DPA support  
- FPGA A to B, B to C, A to C interconnect: >1500 signals each  
- Greatly simplified logic partitioning  
- Synplicity Certify™ models for partitioning assistance  
- 3 separate programmable clock synthesizers (ICS8442)  
  - 3 Global clocks (ACLK, BCLK, CCLK)

Block Diagram

- User configurable via Compact Flash, PCI, or USB  
  - Dedicated 64-bit/66MHz PCI Bridge - QL5064  
  - No FPGA resources consumed for PCI  
  - Maximum PCI data transfer rate: 533mb/s  
  - Programmable Target Prefetching/Write Posting  
  - PCI2.2 Compliant  
  - Zero Wait State Master and Target Bursting  
  - Five Independent Master DMA Channels:  
    - 2 -- Transmit  
    - 2 -- Receive  
    - 1 -- Single PCI Access (SPCI)  
    - DMA Chaining/Scatter Gather  
    - Mailboxes, Interrupts  
  - Advanced FPGA configuration via PCI, USB2.0, or Compact Flash  
  - Partial reconfiguration support on all FPGAs  
  - 3 separate DDR2 SODIMMs (200MHz)  
    - 1 per each FPGA  
    - 64-bit data width, 200MHz operation  
    - PC2-3200/PC2-4200  
    - Addressing and power to support 4GB in each socket  
    - Verilog/VHDL reference design provided (no charge)

- DDR2 SODIMM data transfer rate: 25.6Gb/s  
- Alternate SODIMM’s available (consult factory):  
  - QDR SDRAM  
  - SDRAM pipeline/flowthrough, NoBL/ZBT  
  - FLASH  
  - Micror connectors  
  - Micron RLDRA

- FPGA configuration via PCI, Compact Flash, USB  
- Status LED’s  
- Standalone operation with off-the-shelf ATX power supply.  
- Two, 400-pin expansion connectors with 348+ connections + clocks  
  - Custom daughter cards  
  - Single-ended or LVDS, +2.5/3.3V tolerant  
- Full support for embedded logic analyzers via JTAG interface  
  - SignalTap II  
  - Identify™ from Synplicity

Available Speed Grades

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Available Speed Grades</th>
<th>Slices or LE’s</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Memory (per FPGA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(slowest to fastest)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2S90</td>
<td>-5,-4,-3</td>
<td>36,384</td>
<td>72,768</td>
<td>1,020 (100%)</td>
<td>M512 (32x16)</td>
</tr>
<tr>
<td>2S130</td>
<td>-5,-4,-3</td>
<td>53,016</td>
<td>106,032</td>
<td>1,480 (60%)</td>
<td>M4K (128x36)</td>
</tr>
<tr>
<td>2S180</td>
<td>-5,-4,-3</td>
<td>71,760</td>
<td>143,520</td>
<td>2,010 (60%)</td>
<td>M-RAM (4kx144)</td>
</tr>
</tbody>
</table>

Max I/O’s

<table>
<thead>
<tr>
<th>FF’s in I/O pad</th>
<th>Multiplexers (18x18) B</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>192</td>
</tr>
<tr>
<td>7</td>
<td>252</td>
</tr>
<tr>
<td>7</td>
<td>384</td>
</tr>
</tbody>
</table>

Max M512

<table>
<thead>
<tr>
<th>M512 (32x16)</th>
<th>45,200,448</th>
</tr>
</thead>
<tbody>
<tr>
<td>M4K (128x36)</td>
<td>6,747,840</td>
</tr>
<tr>
<td>M-RAM (4kx144)</td>
<td>9,383,040</td>
</tr>
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</table>
Description

The DN7000K10PCI is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN7000K10PCI is hosted in a 32-bit or 64-bit PCI slot (33/66MHz) or can be used stand-alone. A single DN7000K10PCI configured with 3 of Altera’s 2S180’s can emulate up to >3.6 million gates of logic as measured by LSI. And this number does not include the embedded memories and DSP blocks resident in each FPGA. The DN7000K10PCI achieves high gate density and allows for fast target clock frequencies by utilizing FPGA's from Altera’s StratixII family of FPGA’s. High I/O-count, 1508-pin, flip-chip BGA packages are employed, providing for abundant, fixed interconnect between the FPGA's. All FPGA interconnect is single-ended or differential, with differential clocked up to 500MHz. In addition, the I/O SERDES functionality is thoroughly tested and characterized, allowing for 10x pin multiplying on differential pairs between FPGA’s and dramatically easing the partitioning problem. The industry’s highest performance PCI Bridge, the QL5064, enables data transfer via master-moding and chaining, without making any resource demands on the StratixII FPGA’s. One DDR2 SDRAM SODIMM per FPGA is provided, allowing each FPGA to directly address up to 2GB of memory. Alternative SODIMM’s are available, including QDR SSRAM, SSRAM pipeline/flowthrough, NoBL/ZBT, FLASH, Mictor connectors, and Micron RLDRAM. Each SODIMM socket is tested at 200MHz, and reference designs are provided. A total of 348+ test pins (plus clocks and power) are provided on the bottom of the PWB via two high performance 400-pin expansion connectors. These expansion headers can also be used for logic analyzer-based debugging or for pattern generator stimulus. Custom daughter cards can be mounted to these connectors as a means to interface the DN7000K10PCI to application-specific circuits. Reference material such as DDR2 SDRAM controllers and PCI drivers (with source) is included (in Verilog, VHDL, C) at no additional cost.