The DN7006k10PCIe-8T is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN7006k10PCIe-8T is hosted in an 8-lane PCIe bus (GEN1), but can be used stand-alone and configured via USB and/or Compact FLASH. A single DN7006k10PCIe-8T configured with 6 Altera Stratix3, 3SL340’s can emulate up to 15 million gates of logic as measured by a reasonable ASIC gate counting standard and this number does not include embedded memories and multipliers resident in each FPGA. One hundred percent (100%) of the 3SL340’s FPGA resources are available to the user application. The DN7006k10PCIe-8T achieves high gate density and allows for fast target clock frequencies by utilizing the largest FPGA from Altera’s Stratix3 family. Any subset of FPGA’s can be stuffed and we can accommodate any combination of speed grades.

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Speed Grades (slowest to fastest)</th>
<th>LUT Size</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Multipliers (18x16)</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stratix3</td>
<td>3SL340</td>
<td>6-input</td>
<td>270,000</td>
<td>Max (100% util) (1000’s)</td>
<td>M9K (9 kbit)</td>
<td>M144K (144 kbit)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Practical (60% util) (1000’s)</td>
<td>6750</td>
<td>1040</td>
</tr>
</tbody>
</table>

- 93 LVDS unidirectional pairs + clocks (or 186 single-ended)
- 450MHz on all signals with source synchronous LVDS
- Signal voltage set by daughter card (1.2v to 3.3V)
- Reset
- Supplied power rails (fused):
  - +12v (24W max)
  - +5V (10W max)
  - +3.3V (10W max)
- Pin multiplexing to/from daughter cards using LVDS (up to 10x)

- Fast and Painless FPGA configuration
  - CompactFLASH, USB, PCIe, JTAG
  - Configuration Error reporting
  - Accelerated configuration readback
  - RS232 port for embedded uP debug
  - Accessible from all FPGA’s via separate 2-signal bus
- Full support for embedded logic analyzers via JTAG interface
  - SignalTap, and other third-party debug solutions
- 54 status FPGA-controller LED’s: enough illumination to decontaminate minimally processed vegetables.
Dedicated PCIe, 8-lane controller
We ship the DN7006k10PCIe-8T with a full function, fixed, 8-lane master/target. Drivers and ‘C’ source for several operating systems are included at no cost.

Stratix3 FPGAs from Altera
The DN7006k10PCIe-8T uses high I/O-count, 1760-pin, flip-chip BGA packages. The 3SL340 has 1,120 I/O’s and all are utilized. Abundant fixed interconnects (either differential or single-ended) are provided between the FPGA’s. Where possible, FPGA to FPGA busses are routed and tested LVDS, run at 600MHz+ (which is 1.2 Gb/s if used in DDR mode). Single-ended at the reduced speed of 225MHz is characterized and tested. Example designs utilizing the integrated I/O shift registers with DDR for pin multiplexing are included. A 96-pin main bus (MB) is connected to all FPGAs including the configuration FPGA. The connection to the configuration FPGA allows for data movement via USB to any/all FPGA’s.

Daughter cards
Three separate 400-pin FCI MEG-Array connectors allow for customization with daughter cards. Where possible, signals to and from these cards are routed differentially and can run at the limit of the FPGA: 450MHz. Clocks, resets, and presence detection, along with abundant power are included in each connector. Two adjacent MEG-Array connectors can be converted to FPGA to FPGA interconnect with a DNMEG_Intercon.

Memory
Four separate DDR2 SODIMM sockets are stuffed and have connections to FPGA’s A, C, D, and F. Each socket is tested to 250MHz with a DDR2 SODIMM. Standard, off-the-shelf DDR2 memory DIMM’s (PC2-4200 or better) work nicely and we can provide these for a small charge. We have developed alternative SODIMM’s that can be stuffed into these positions. Consult the factory for more details, but the list includes FLASH, SSRAM, QDR SSRAM, mictors, USB PHYs, DDR3, and others.

Easy Configuration via Compact FLASH, PCIe or USB
The configuration bit files for the FPGA's are copied onto a Compact FLASH card (provided) and an on-board Cypress microprocessor controls the FPGA configuration process. FPGA configuration can also be controlled via the USB interface or downloaded via PCIe. Visibility into the configuration process is enhanced with an RS232 port. Sanity checks are performed automatically on the configuration bit files, streamlining the configuration process. FPGA configuration occurs at the fastest possible parallel frequency. FPGA configuration is quick and painless. Multiple LED’s provide instant status and operational feedback. As always, reference material such as a DDR2 SDRAM controller is included (in Verilog, VHDL) at no additional cost.

Status LED’s, Debug
Although no specific testing was performed, sophisticated statistical finite element models are showing that the dozens of status LED’s provide enough illumination to decontaminate minimally processed vegetables. More info here: Decontaminating Food with Light. Please don’t try this at home since the risk is high. These LED’s are user controllable from the FPGA’s so can be used as visual feedback in addition to sanitizing rotten veggies. A JTAG connector provides an interface to SignalTap and other third party debug tools. Other FPGA debug solutions will be available later in ‘08.
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