Features

- PCI Express (8-lane) logic prototyping system with 2-6 Altera Stratix-4 FPGAs
  - EP4SE820-3, -2 (slowest to fastest)
  - EP4SE530-3, -2
- FF1760 package: 1,120 I/Os (with 4SE820)
- Fixed 8-lane PCIe interface and controller provided
  - PCIe GEN1 rev 1.1
  - PCIe GEN2 with upgrade
- 40+ million ASIC gates (ASIC measure) when stuffed with 6 Stratix-4 4SE820s
- FPGA to FPGA interconnect is a mix of single-ended and LVDS
  - 600 MHz LVDS chip to chip (1.2 Gb/s)
  - LVDS pairs can be used as two single-ended signals at reduced frequency (~225MHz)
  - Reference designs for integrated I/O pad ISERDES/OSERDES
  - 10x pin multiplexing per LVDS pair
  - Greatly simplified logic partitioning
  - Source synchronous clocking for LVDS
- Main Bus (MB) connects all Stratix-4 FPGAs (96 signals)
  - Single-ended
- Auspy models for partitioning assistance
- 4 separate DDR2 SODIMMs (350MHz)
  - Direct connection to FPGAs A, C, F, D
  - PC2-4200 or better
  - Addressing/power to support 4GB in each socket
  - DDR2 Verilog/VHDL reference design provided (no charge)
  - DDR2 SODIMM data transfer rate: 32Gb/s
  - Alternate pin compatible memory cards available (consult factory for availability):
    - SRAM: QDR, ASYNC, STD, or PSRAM, FLASH
    - DRAM: SDR, DDR1, PSRAM or RLDRAM, DDR3
- Mictor, USB PHY, Extra Interconnect
- Seven independent low-skew global clock networks
  - G0, G1, G2, M48, EXT0, EXT1, REF
- Three, high-resolution, user-programmable synthesizers for G0, G1, G2
- User configurable via CompactFLASH, USB, and/or PCIe
- All seven global clocks networks distributed differentially and balanced
- Two independent single-step clocks
  - Seven independent external clocks inputs (single-ended or differential) can be injected onto low-skew global clock networks
- Flexible customization via daughter cards using expansion connectors
  - 3 daughter card locations: FPGAs D, E, F
  - 400-pin FCI MEG-Array connectors
  - 93 LVDS unidirectional pairs + clocks (or 186 single-ended)
  - 450MHz on all signals with source synchronous LVDS
  - Signal voltage set by daughter card (1.2v to 3.3V)
  - Reset
  - Supplied power rails (fused):
    - +12v (24W max)
    - +5v (10W max)
    - +3.3v (10W max)
- Pin multiplexing to/from daughter cards using LVDS (up to 10x)
- Fast and Painless FPGA configuration
  - CompactFLASH, USB, PCIe, JTAG
  - Configuration Error reporting
  - Accelerated configuration readback
- RS232 port for embedded uP debug
  - Accessible from all FPGAs via separate 2-signal bus
- Full support for embedded logic analyzers via JTAG interface
  - SignalTap, and other third-party debug solutions
- 54 status FPGA-controller LEDs: bright enough to illuminate airplane landing strips

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<th>LUT Size</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Max I/O’s</th>
<th>Multiwire (16x18)</th>
<th>Memory</th>
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<td>656,000</td>
<td>10,496</td>
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<td>960</td>
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<td>270,000</td>
<td>4,320</td>
<td>2,592</td>
<td>1120</td>
<td>576</td>
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The Dini Group
DN7406K10PCIe-8T
ASIC Prototyping Engine Featuring Altera Stratix IV
Hosted via 8-lane PCI Express (GEN1/GEN2)
Block Diagrams

DN7406K10PCIe-8T (with 4SE820)

DN7406K10PCIe-8T (single ended with 4SE820)
DN7406K10PCIe-8T ASIC Prototyping Engine Featuring Altera Stratix IV

DN7406K10PCIe-8T (with 4SE530)

DN7406K10PCIe-8T (single ended with 4SE530)
Description

Overview

The DN7406k10PCIe-8T is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN7406k10PCIe-8T is hosted in an 8-lane PCIe bus (GEN1), but can be used stand-alone and configured via USB and/or Compact FLASH. A single DN7406k10PCIe-8T configured with 6 Altera Stratix IV, 4SE820’s can emulate up to 40 million gates of logic as measured by a reasonable ASIC gate counting standard and this number does not include embedded memories and multipliers resident in each FPGA. One hundred percent (100%) of the 4SE820’s FPGA resources are available to the user application. The DN7406k10PCIe-8T achieves high gate density and allows for fast target clock frequencies by utilizing the largest FPGA from Altera's Stratix IV family. Any subset of FPGA’s can be stuffed and we can accommodate any combination of speed grades in any FPGA position.

Dedicated PCIe, 8-lane controller (GEN1, GEN2 with upgrade)

We ship the DN7406k10PCIe-8T with a full function, fixed, 8-lane master/target. Drivers and ‘C’ source for several operating systems are included at no cost.

Stratix IV FPGAs from Altera

The DN7406k10PCIe-8T uses high I/O-count, 1760-pin, flip-chip BGA packages. The 4SE820 has 1,120 I/O’s and all are utilized. Abundant fixed interconnects (either differential or single-ended) are provided between the FPGAs. Where possible, FPGA to FPGA busses are routed and tested LVDS, run at 600MHz+ (which is 1.2 Gb/s if used in DDR mode). Single-ended at the reduced speed of 225MHz is characterized and tested. Example designs utilizing the integrated I/O shift registers with DDR for pin multiplexing are included. A 96-pin main bus (MB) is connected to all FPGAs including the configuration FPGA. The connection to the configuration FPGA allows for data movement via USB to any/all FPGA’s.

The 4SE530 is also applicable, but make sure you understand the interconnect lost with the reduced pin count of this device.

Daughter cards

Three separate 400-pin FCI MEG-Array connectors allow for customization with daughter cards. Where possible, signals to and from these cards are routed differentially and can run at the limit of the FPGA: 600 MHz. Clocks, resets, and presence detection, along with abundant power are included in each connector. Two adjacent MEG-Array connectors can be converted to FPGA to FPGA interconnect with a DNMEG_Intercon.
Memory

Four separate DDR2 SODIMM sockets are stuffed and have connections to FPGAs A, C, D, and F. Each socket is tested to 350MHz with a DDR2 SODIMM. Standard, off-the-shelf DDR2 memory DIMM’s (PC2-4200 or better) work nicely and we can provide these for a small charge. We have developed alternative SODIMMs that can be stuffed into these positions. Consult the factory for more details, but the list includes FLASH, SSRAM, QDR SSRAM, mictors, USB PHYs, DDR3, and others.

Easy Configuration via Compact FLASH, PCIe or USB

The configuration bit files for the FPGAs are copied onto a Compact FLASH card (provided) and an on-board Cypress microprocessor controls the FPGA configuration process. FPGA configuration can also be controlled via the USB interface or downloaded via PCIe. Visibility into the configuration process is enhanced with an RS232 port. Sanity checks are performed automatically on the configuration bit files, streamlining the configuration process. FPGA configuration occurs at the fastest possible parallel frequency. FPGA configuration is quick and painless. Multiple LEDs provide instant status and operational feedback. As always, reference material such as a DDR2 SDRAM controller is included (in Verilog, VHDL) at no additional cost.

Status LEDs, Debug

Although no specific testing was performed, sophisticated statistical finite element models and back of the envelope calculations are showing the dozens of status LED’s to be bright enough to illuminate a large airplane jet runway. Please don’t try this at home since the risk is high and the dangers great. These LEDs are user controllable from the FPGAs so can be used as visual feedback in addition to airline runway illumination. A JTAG connector provides an interface to SignalTap and other third party debug tools.
For technical applications and sales support, call 858.454.3419

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