Errata for DN7406K10PCIe-8T PWB Assembly

This document describes all errata that apply to DN7406K10PCIe-8T PWB Assemblies. Both revision 1 and revision 2 are covered; when errata applies to only one revision, it will be noted as such.

1 Revision History
2011-01-25 – Added Temperature Sensor Errata

2 Temperature Sensors May Read Back Invalid Values Under High Load Conditions

2.1 Summary of Problem
Under high-load, high I/O toggle rate conditions, the on-board temperature sensors that measure the core temperature of the FPGAs may malfunction and read back an incorrect temperature value. This behavior is caused primarily by noise coupling onto the external temperature diode lines inside of the Stratix-III/Stratix-IV FPGAs. As Altera describes in the Stratix-III user manual,

The TSD is a very sensitive circuit which can be influenced by the noise coupled from traces on the board, and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on milivolts of difference as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends you take temperature readings during periods of no activity in the device (for example, standby mode where no clocks are toggling in the device), such as when the nearby I/Os are at a DC state and the clock networks in the device are disabled.

Due to the potential for noise coupling onto the external temperature sensor pin connections, the MCU may read back an erroneously high temperature and clear the FPGAs, even though they are in reality not overheating.

2.2 Product Behavior
While running the FPGAs with a user design, the FPGAs may suddenly be cleared. The MCU will output a message on the MCU RS232 port reflecting this. If the temperature reported by the MCU is around 85 degrees (the default reset threshold) then it is potentially valid and the FPGAs are in reality overheating. If the temperature reads back a very high value, or an FPGA that isn't even configured and/or under load is reported to be overheating, the temperature is potentially being misread. In this case the FPGAs might not be overheating. This behavior is symptomatic of the temperature sensor problem described in this errata.

2.3 Work-Around
If the user has determined that the temperature sensor data is being read back incorrectly, then it is possible to disable the temperature sensor readback and thus prevent the MCU from clearing the FPGAs
when the temperature sensors are read back incorrectly. The over-temperature reset can be disabled via the MCU RS232 interface by setting the reset threshold temperature to +127. This requires connecting to the board via an RS232 terminal. The procedure for this is split across two sections in the DN7406K10PCIe-8T user manual, section 3.1 and 3.3.

As a safety precaution, when disabling the over-temperature reset, it is recommended that the user use the internal temperature sensor to monitor FPGA temperature. In Altera Stratix-III and Stratix-IV FPGAs, the ALTTEMP_SENSE Megafunction can be used to read the temperature from the internal temperature sensor. It is left up to the user to make use of this temperature data; several possible implementations include setting an error flag and halting the user design when a dangerous temperature is reached, or simply allowing the temperature to be read back via the Mainbus FPGA interface. The internal sensor has not been found to suffer from the same problems as the on-board sensor and can be used to gauge whether the FPGA is overheating. It is also possible to use the internally measured value to determine whether the on-board external temperature sensor is reading an accurate value for the FPGA core temperature, or whether the external sensor is suffering from inaccuracy due to high FPGA load.

**Note that the Stratix-III FPGAs do not support use of the internal temperature sensor. This is covered in the latest Stratix-III errata.**