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1. Introduction

The Triton design can be partitioned into two functional sections, the “array section,” and the “configuration section.” The array section contains sixteen, Virtex4 FPGAs (also referred to as “V4”), which are used for logic emulation. The configuration section contains a single Virtex4 FPGA and a microcontroller. The configuration section implements a user interface, configures the array FPGAs, and controls system clocking resources.

Figure 1.1 illustrates a high-level block diagram for the Triton board.

![Triton High-Level Block Diagram](image)

1.1 Array Section Overview

The array section consists of a four-by-four array of Xilinx Virtex4 FPGAs, containing fourteen “LX” type chips and two “FX” type chips. The FX parts contain “RocketIO” Multi-Gigabit Transceivers (MGT), which are used to implement high-speed serial links.

A “lattice” interconnect structure is used to interconnect neighboring FPGAs in the array using high-speed, point-to-point links.

A “main bus” interconnect structure is used to interconnect all FPGAs in the array, as well as to the FPGA in the configuration section.

FPGAs on the periphery of the array include either a daughter card interface, or a memory expansion interface.

Figure 1.2 is a high-level block diagram for the array section, including the lattice interconnect.

Figure 1.3 is a high-level representation of the main bus.
Figure 1.2 Triton Array Section High-Level Block Diagram with Peripherals and Lattice Interconnect
1.2 Configuration Section Overview

The configuration section implements a small micro-controller, which is used to implement a user interface and provide control and management for the board. User interfaces include a high-speed USB interconnect, multiple RS-232 ports, and a remote I/O interface, which is used to connect to I/O devices on the chassis front panel. A daughter card interface is provided for user I/O expansion. The microprocessor can access several types of media cards, including Smart Media, Compact Flash, and a remote, Compact Flash drive, located on the chassis front panel.

Array section connections include configuration busses to each of the array FPGAs, a “Main Bus” connection, control and status lines, global clocks, and I/O expansion CPLDs, which are distributed throughout the array section.

Figure 1.4 is a high-level block diagram for the configuration section.
1.3 Revision History

Please use the following format for version updates:

<version>, <initials>, <date>, <description>

V1.0, GR, 8/12/05, first release
2. Inter-FPGA Interconnect

The inter-FPGA interconnect consists of short, point-to-point, high-speed serial, differential links between adjacent FPGAs in the array section. These links are designed to use LVDS signaling. Interconnects are organized on a bank-to-bank basis, i.e., one full bank on one FPGA is interconnected with one full bank on the adjacent FPGA. It is expected that users will multiplex these interconnects when logical signaling requirements exceed the physical interconnect capacity.

2.1 Interconnect Description

Figure 2.1 is a block diagram for the inter-FPGA interconnect to be used on the Triton board. Items to note include the following:

- This diagram illustrates the physical bank structure of the interconnected FPGAs. Each arrow on the diagram represents a full, bank-to-bank interconnect, which consists of 31 differential pairs.
- The FPGAs in the array are assigned numbers from 0 to 15, which are applied in row-major order. These parts are also referred to as F0 through F15.
- The FPGA in the configuration section is assigned number 16, and is also referred to as F16.
- The daughter card connectors associated with the FX60/100 chips do not contain bank interconnects due to the priority of maintaining the inter-FPGA interconnects while using the smaller FX parts.
- The asymmetry in the north-south interconnect between FPGAs 7 and 11 is due to the use of larger daughter card connectors on those parts.
- Daughter card connectors are arranged as banks, which reflect the organization of the Virtex4 bank structure. Two sizes of connectors are used, a 300-pin connector, which fits two V4 banks, and a 400-pin connector, which fits three V4 banks. The corner FPGAs, F3 and F15, implement five banks of daughter card interconnects by using both 300-pin and 400-pin connectors.
Figure 2.1 Inter-FPGA Lattice
3. Main Bus

The main bus consists of a 144-bit bus, which interconnects all of the FPGAs in the array section. This bus is logically divided into two sub-busses, one which contains 80 bits and the other which contains 64 bits. Single-ended, LVCMOS signaling is used on this bus.

The main bus is also connected to the FPGA in the array section. However, due to pin limitations, the 64-bit bus is connected to banks available only on the LX80 or higher FPGAs. These alternate parts are otherwise pad-compatible with the smaller LX40, which is the default part used. A user who requires the full, 144-bit main bus connection in the configuration section will need to install the larger V4 part.

Transmission gate type bus switches are used to create sub-sections on each bus, which can be independently configured. A vertical “trunk” bus is routed in the configuration section, and can be selectively connected to horizontal bus segments in the array section. The 80-bit bus contains two horizontal segments, while the 64-bit bus contains three horizontal segments. Each segment can be electrically connected to the trunk bus with byte resolution. Segment configuration is controlled by the config MCU.

3.1 Main Bus Description

Figure 3.1 is a block diagram for the main bus interconnect to be used on the Triton board. Items to note include the following:

- This diagram illustrates the physical bank structure of the interconnected FPGAs. The arrows on the diagram represent approximate bank connections to the FPGAs.
- The FX parts do not include connections to the 64-bit bus segments 1 and 3 due to a reduced number of pins available on the banks used for bus interconnect.

Figure 3.2 presents more detail on the main bus bank interconnects within the array section.
Figure 3.1 Main Bus Structure
Figure 3.2 Array Section Main Bus Structure Detail
4. Clocking

Eight global clock trees are included in the design. Four of these clock trees are associated with clocks that are sourced from the configuration section. The remaining four clock trees are used to provide global clock access for the daughter card connectors. Global clocks are implemented using LVDS signaling.

Figure 4.1 provides an overview of the Triton clocking structure.
Figure 4.1 Triton Clocking Structure
4.1 Configuration Section Array Clocks

Four global clocks are sourced from the configuration section. Three of these clock phases are fully configurable from a variety of sources. One additional clock phase is supplied as a “reference clock,” which is driven only from one, synthesized source.

4.1.1 Fully Configurable Global Clocks

Three, fully-featured global clock phases are sourced from the configuration section. These three clocks can be independently sourced from:

- LVDS synthesizer chips, configured by the MCU.
- External clock sources, received using SMA connectors.
- The configuration FPGA, which can provide divided clocks from the synthesizers or a gated, “single-step” clock sourced from a state machine.

The global clocks can support a high-speed “array synchronous” operation, in which all sixteen array FPGAs are synchronously clocked, or a slower-speed “global synchronous” mode, in which the array FPGAs as well as the configuration FPGA are synchronously clocked. The latter mode can be used for data transfer between the configuration and array sections using the main bus.

Figure 4.2 is a block diagram for one phase of the fully configurable configuration section global clocks. Also see section 4.6.

4.1.2 Reference Global Clock

One additional global clock phase is sourced from the configuration section. This clock is referred to as the “reference clock,” and is primarily intended to provide a 200MHz clock source for use with the Virtex4 IDelayCTRL blocks. However, the traces from the 1-to-16 fan out buffer used to distribute the reference clock are length-matched, so the reference clock can also be used for array synchronous operation. Figure 4.3 illustrates the reference global clock.
4.1.3 Configuration Section Global Clock Distribution

Figure 4.4 illustrates the 1-to-16, LVDS fan-out buffer connection, which is used to provide a low-skew set of global clocks to the array FPGAs.
4.2 Daughter Card Array Clocks

Four global array clock trees are provided, which can be used to source clocks from the daughter card connectors in the array section. Clocks from two, adjacent daughter card connectors are multiplexed onto each clock tree.

Figure 4.5 illustrates the manner in which the daughter card clocks are multiplexed and distributed in the array section. Note that there is no connection from the daughter card clocks to the configuration FPGA.
Figure 4.5 Daughter Card Clock Multiplexing and Distribution
4.2.1 Daughter Card Array Clock Distribution

One application for the daughter card clocks is target clock sourcing during logic emulation. In this configuration, the Triton board is connected to the target system via the daughter card connectors, and the target system provides the synchronous clock for the “ASIC,” which is emulated within the array FPGAs. Due to this, a “zero-skew” clock distribution network is required for the daughter card clocks. This is implemented using PLL-type, zero-delay clock distribution buffers. Figure 4.6 illustrates one of the four clock trees used for daughter card clock distribution.

Figure 4.6 Daughter Card Clock Distribution

4.3 Daughter Card Local Clocks

Each daughter card connector also provides two local clocks, which are connected to the associated FPGA. These clocks can be used to provide phase reference feedback from the daughter card to a DCM in the FPGA. Since the Virtex4 parts divide their center column (which contains the DCMs) into a “top half” and a “bottom half,” two local clocks are provided to allow the daughter card to directly interface to clocking resources located in either half of the column.

Figure 4.7 illustrates the daughter card local clock connection.
4.4 Configuration Clocks

All sixteen FPGAs in the array section have point-to-point CCLK connections, which are used for configuration purposes. These sixteen clocks are sourced from the configuration FPGA.

Figure 4.8 illustrates the configuration clock structure.
4.5 SO-DIMM Clocks

Globally synchronous clocks for the SO-DIMM memory expansion interfaces are generated in the associated FPGA and distributed to the SO-DIMM connector using an external clock buffer. A phase reference feedback clock is used to produce a synchronous clock for the FPGA interface logic.

Figure 4.9 illustrates the SO-DIMM clock generation circuit.

![Figure 4.9 SO-DIMM Clock Generation and Distribution](image)

4.6 Configuration Section Clocks

The daughter card connector in the configuration section cannot directly source an array global clock. Instead, it connects all three of its daughter card clocks as local clocks.

Figure 4.10 provides details on the connection of clocks to and from the configuration section FPGA. Note that all three phases of the fully-configurable global clock are represented in this diagram.
Figure 4.10 Configuration Section FPGA Clocks
5. Configuration Section

Figure 5.1 provides a block diagram for the configuration section. Primary differences in the Triton design relative to earlier Dini Group emulator designs include the following:

- Substitution of a LX40 FPGA for the Spartan II FPGA.
- A Compact Flash interface in addition to the usual Smart Media interface.
- A remote Compact Flash drive interface to access a chassis-mounted CF drive.
- A high-density daughter card connector.
- A remote display interface.

Figure 5.1 Configuration Section Block Diagram

Figure 5.2 illustrates the bank assignments for the LX40/80 part in the configuration section. Note that the 64-bit main bus is connected to banks that are only present in the LX80 and up parts.
5.1 Array Configuration Interface

The connections for array FPGA configuration (i.e., connections to bank 0 signals in the array FPGAs) are primarily point-to-point, with only a few bussed signals. The bussed configuration interconnect (multiple slave device SelectMAP configuration), as illustrated in the Xilinx V4 configuration guide, is not used due to problems experienced on previous Dini Group emulators with configuration. Bussed signals are implemented in four, separate busses, which run horizontally through the rows in the array section.

Figure 5.3 illustrates a configuration interface “block,” which represents I/O signals associated with one row of the array. Four of these signal blocks are used to interconnect with the sixteen FPGAs in the array section. As shown, BUSY and DATA[7:0] are the only bussed signals in each of the four interfaces.
5.2 Config Section FPGA Configuration

The FPGA in the configuration section is itself configured using a Xilinx configuration PROM device.
6. CPLD I/O Expansion

Due to the large number of control lines associated with the clock synthesis and distribution parts used in the array section, a group of I/O expansion CPLDs are used to extend the scope and reach of the configuration section I/O to these parts. I/O on these CPLDs is accessed by the MCU via a serial interface. These CPLDs are programmed using a separate JTAG chain.

In addition, two of the CPLDs provide I/O expansion for the two FX parts, which require status and control connections to several of the high-speed serial I/O interfaces, including the XFP and SFP modules.

Figure 6.1 provides an overview of the I/O expansion CPLD locations and JTAG chain arrangement.

![Figure 6.1 I/O Expansion CPLD Locations and JTAG Chain](image)

Table 6.1 provides a summary of I/O connectivity provided by each of the I/O expansion CPLDs. Note that signals assigned to the CPLDs for MCU access are biased toward “set-and-leave” type configuration signals, which are generally accessed only when a clocking configuration is being set. Read-back status signals for the power regulators will be accessed only at reset events. Serial communications lines for the RocketIO clock synthesizers are sourced directly from the configuration FPGA.

FX-accessed functions, which consist of XFP and SFP ports, are connected to the FX CPLDs to free FPGA I/O on F0 and F12 to be used for inter-FPGA, main bus, and daughter card interconnects. However, XFP 2-wire serial interfaces are sourced directly from the FPGAs.
<table>
<thead>
<tr>
<th>CPLD Name</th>
<th>MCU Accessed Functions</th>
<th>FX Accessed Functions</th>
</tr>
</thead>
</table>
| Q0 (Quadrant 0) | • Control of leaf-level, zero-delay buffers in daughter card global clock trees.  
|  | • Monitoring of power regulator comparator outputs: +1.2V_0, +1.2V_1, +1.2V_4, +1.2V_5,  
|  | +2.5V_0, +2.2V | None |
| Q1 (Quadrant 1) | • Control of leaf-level, zero-delay buffers in daughter card global clock trees.  
|  | • Monitoring of power regulator comparator outputs: +1.2V_2, +1.2V_3, +1.2V_6, +1.2V_7,  
|  | +2.5V_1, +1.8_0 | None |
| Q2 (Quadrant 2) | • Control of leaf-level, zero-delay buffers in daughter card global clock trees.  
|  | • Monitoring of power regulator comparator outputs: +1.2V_10, +1.2V_11,  
|  | +1.2V_14, +1.2V_15, +1.2V_16, +2.5V_2, +1.8_1 | None |
| Q3 (Quadrant 3) | • Control of leaf-level, zero-delay buffers in daughter card global clock trees.  
|  | • Monitoring of power regulator comparator outputs: +1.2V_8, +1.2V_9, +1.2V_12,  
|  | +1.2V_13, +2.5V_3 | None |
| CNTR (Center) | • Control of top-level, zero-delay buffers in daughter card global clock trees. Tree buffer master resets. Daughter card clock multiplexer selects.  
|  | • Power-up detector | None |
| FX0 (RIO top) | • Control of RIO clock synthesizers and multiplexers. | • Control and status I/O for XFP and SFP modules. |
| FX1 (RIO bottom) | • Control of RIO clock synthesizers and multiplexers. | • Control and status I/O for XFP and SFP modules. |

Table 6.1 I/O Expansion CPLD Functions
7. RocketIO Subsystem

The FX parts are used to implement multiple channels of high-speed serial I/O. The FX60/100 used on Triton provides either 16 (FX60) or 20(FX100) MGT channels per corner of the board. High-speed I/O connections provided include the following:

- **XFP** – used for high-speed (10Gbps) optical modules, two per corner of board.
- **SFP** – used for medium-speed optical modules, two per corner of board.
- **End-launch SMA** – two channels of high-speed I/O are implemented per FX using end-launch SMA connectors, which have optimized microstrip interfaces and are accessed directly through the back plate of the chassis.
- **Straight SMA** – two channels of medium-speed I/O are implemented per FX using straight SMA connectors. These parts present an inductive impedance discontinuity in the PWB interface, which is expected to limit their frequency of operation. These ports are accessed using bulkhead SMA connectors in the back plate, with jumper cables to the PWB.
- **Daughter card connectors** – the 300-pin daughter card connectors associated with each FX part provide four MGT channels per corner of the board. These interfaces are expected to support medium- to high-speed serial I/O links.
- **Samtec connectors** – these small, differential, coaxial ribbon connectors will be used for general-purpose serial I/O expansion. A “primary” Samtec connector will always be loaded at each corner of the board. This connector will carry four MGT channels. A “secondary” Samtec connector will be loaded at each corner of boards that load FX100 parts. The secondary connector, if loaded, will carry four MGT channels.

7.1 RocketIO Clocking Configurations

The MGT “tiles” on the FX parts are organized as two “columns.” Four MGT reference clock inputs are provided by the part, two per column. Note that a reference clock input on one column cannot clock MGT tiles on the opposite column.

MGT reference clock sources include two, low-jitter, synthesized clocks, two oscillator modules, and one daughter card sourced clock. The following sections detail how these clocks are arranged and multiplexed for the two types of boards.

7.1.1 MGT Clocking Description

Figure 7.1 illustrates MGT clocking for the Triton board.
Figure 7.1  MGT Clocking for Triton
7.2 MGT Tile Assignments

The following section details the mapping of serial I/O interfaces to MGT tiles on the FX part.

7.2.1 MGT Tile Mapping

<table>
<thead>
<tr>
<th>“Right” Column Tiles</th>
<th>Functional Assignment</th>
<th>“Left” Column Tiles</th>
<th>Functional Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>109</td>
<td>Daughter card channels 3 and 4</td>
<td>101</td>
<td>Samtec channels 5 and 6 (FX100 only)</td>
</tr>
<tr>
<td>110</td>
<td>XFP Modules (CHA non-functional)</td>
<td>102</td>
<td>Samtec channels 3 and 4</td>
</tr>
<tr>
<td>112</td>
<td>Daughter card channels 1 and 2</td>
<td>103</td>
<td>Samtec channels 1 and 2</td>
</tr>
<tr>
<td>113</td>
<td>SFP modules</td>
<td>105</td>
<td>Straight SMA connector pairs</td>
</tr>
<tr>
<td>114</td>
<td>Samtec channels 7 and 8 (FX100 only)</td>
<td>106</td>
<td>End-Launch SMA connector pairs</td>
</tr>
</tbody>
</table>

Table 7.1 RocketIO Tile Assignments for FPGA 0 (FX60/100)

<table>
<thead>
<tr>
<th>“Right” Column Tiles</th>
<th>Functional Assignment</th>
<th>“Left” Column Tiles</th>
<th>Functional Assignment</th>
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<tr>
<td>109</td>
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<td>114</td>
<td>Samtec channels 7 and 8 (FX100 only)</td>
<td>106</td>
<td>Samtec channels 1 and 2</td>
</tr>
</tbody>
</table>

Table 7.2 RocketIO Tile Assignments for FPGA 12 (FX60/100)
7.3 MGT Tile Positions on FX Parts

The following section describes the physical location of the MGT tiles on the FX parts. Note that each tile implements two RocketIO channels, each of which consists of one receive differential pair and one transmit differential pair.

7.3.1 MGT Tile Locations

Figure 7.3 illustrates the MGT tile locations on the FX60/100 part.
7.4 High-Speed Serial I/O Placement and MGT Routing

The following section describes the placement of the serial I/O at each corner of the board and the associated routing to the MGT tiles on the FX parts. Note that mirror-image symmetry is used for placement of the serial I/O connectors on the top and bottom of the board. However, the FX tile placements are fixed on the chip, so MGT tile assignments must differ between the top and bottom portions of the board in order to optimize high-speed serial routing.

7.4.1 Serial I/O Placement and MGT Routing

Figure 7.5 illustrates serial I/O placement and routing for the top corner of the board.
Figure 7.6 illustrates serial I/O placement and routing for the bottom corner of the board.
7.5 XFP Reference Clock

The XFP specification requires that a “reference clock” be provided, which runs at 1/64th the baud rate of the interface. Figure 7.8 illustrates a reference clock receiver, which will be used to supply the XFP reference clock to the modules, if required. Note that a daughter card interface is required to use this arrangement.

Figure 7.8 XFP Reference Clock Generation and Receiver Circuit
8. Daughter Card Interface

The daughter card interface makes use of 300-pin and 400-pin MEG-Array connectors, which are manufactured by FCI. The Triton board mounts four, 300-pin connectors on the left side of the array, and four 400-pin connectors on the right-side of the array. Two additional 300-pin connectors are used on the right side of the array on the corner FPGAs. One, 300-pin connector is used in the configuration section.

Connections provided by each daughter card include the following:

- Two (300-pin) or three (400-pin) full Virtex4 bank interconnects. Each bank consists of 62 connections, which can be used single-ended, or as a loosely-coupled, differential pair.
- Three dedicated, differential clock connections. This interface is used to source clocks from the daughter card to the motherboard.
- Power connections. Three voltage rails are provided by the motherboard to the daughter card, including +12V, +5V, and +3.3V.
- Bank VCCO power. FPGA VCCO power is provided by the daughter card for each connected bank. This allows the daughter card to define the I/O standard to be used on the bank.
- Mother board reset is buffered and driven open-drain to the daughter card.
- Optionally, RocketIO signals are driven on dedicated differential-pair connector pins for daughter cards associated with FX parts.

The daughter card connectors are mounted on the back-side of the Triton motherboard to avoid clearance issues with top-side parts. Figure 8.1 illustrates the connector mounting arrangement.

![Figure 8.1 Daughter Card Mounting Arrangement](image)

The daughter card receptacle on the daughter card itself will also be mounted on the back side of the board. Figure 8.2 illustrates the trace and via topology that results from this connector arrangement.
8.1 Daughter Card Pin Assignments

Figure 8.3 provides a graphic representation of the pin assignments for the 300- and 400-pin connectors. Note that this is a view from the back-side of the connector. Note that the green boxes represent ground connections.

Items to note include the following:

- The first 300 pins on both connectors are identical. This should allow a 300-pin connector to be installed on a 400-pin land pattern on a daughter card to allow limited functionality in 300-pin daughter card positions.
- The central columns use a closely-coupled, differential pair pin arrangement, which is uniformly surrounded by ground pins. Adjacent, diagonal signals can also be defined as “logic-low” in order to completely surround these pins with ground potential. These differential pins are used for RocketIO connections on FX parts.
- All other signals use a “checkerboard” type of ground arrangement. This allows the signals to be used as high-speed, single-ended, or as loosely-coupled differential pairs.
- Two VCCO pins are used per bank for interconnect redundancy.
Figure 8.3 Pin Assignments for 300- and 400-Pin Daughter Card Connectors
8.2 VCCO Bias Generation

Since a daughter card will not always be present on a daughter card connector, a VCCO bias generator is used on the motherboard for each daughter card bank. It is believed that the VCCO pins must be biased in order to correctly initialize the FPGA. The VCCO bias generators supply +1.2V to the VCCO pins on the FPGAs, and are back-biased by the daughter card when it drives the VCCO rails.

8.3 Daughter Card Locations

Please see the “Board Physical” section.
9. Memory Expansion Interface

Four, memory expansion interfaces are provided on the Triton motherboard in the array section. These interfaces make use of the standard SO-DIMM connector interface, which is designed to accept DDR2 memory modules. The Triton board will accept standard DDR memory modules, but it can also optionally be configured to accept non-standard modules, which may contain SRAM or EPROM. These non-standard modules may require rail voltages higher than +1.8V.

An adjustable power regulator is used to provide power for the two memory interfaces located at the top of the array. A separate, adjustable power regulator is used for the two memory interfaces located at the bottom of the array. Each of these regulators can be configured to supply the standard, +1.8V, or, optionally, +2.5V, or +3.3V for non-standard modules. Voltage adjustment is accomplished by adding a trim resistor, which is mounted on the top side of the board. Regulator output will be +1.8V if no trim resistor is present. If a voltage greater than +1.8V is configured, a red LED will illuminate to provide visual feedback regarding the non-standard memory connector power voltage. However, since a user will install a memory module while the system power is off, a warning sticker will need to be used to help prevent a user from destroying a standard DDR2 module if the interface voltage is set to a non-standard value.
10. Power, Cooling, and Reset

The Triton motherboard will be powered by a Zippy H1M-6607P, 600W, 1U height, server-type power supply. This supply can provide up to 48A at 12V, 30A at 5V, and 24A at 3.3V (not simultaneously, however – aggregate limit is 600W). The Triton motherboard will use the +12V rail for its power regulators, which should represent the bulk of the power draw for the system. The board will also use the 5V and 3.3V rails, but to a much lesser extent.

Twenty-four, switch-mode power regulators are used on the Triton motherboard to generate FPGA VCCINT power (+1.2V, seventeen regulators, one per V4 FPGA), FPGA VCCO power (+2.5V, four regulators, one per quadrant), memory expansion power (+1.8V to +3.3V, two regulators, one per two interfaces), and MGT power (+2.1V, post-regulated to +1.1V using linear regulators).

Each regulator is monitored using a comparator. Outputs from these comparators are “wire-OR’ed” onto a power monitoring bus line, which is monitored by the reset supervisory circuit. Transition detectors will be implemented within the CPLDs to allow the MCU to detect a “brown-out” condition on a particular regulator.

Figure 10.1 illustrates the Triton +12V power subsystem.
Figure 10.1 Triton +12V Power Subsystem
10.1 Cooling

Each of the seventeen V4 FPGAs is cooled using a heat sink/fan assembly. These assemblies are mounted to the PWB to avoid placing mechanical stress on the BGA top cases. The selected assembly has a theta-ca rating of 1.2 deg. C per W, which should allow total device dissipation of 27W at 50 deg. C ambient with a max junction temperature of 85 deg. C.

The chassis also features two cooling fans mounted to the front panel, which exhaust out the back panel. These fans are required when running the Triton motherboard within the enclosure.

10.2 Reset Configuration

The system reset configuration implements the following reset policies:

- If any regulator output is below threshold, the board system reset will be held asserted. This is accomplished by connecting all regulator monitor comparators onto a “wired-OR” bus line, which is sensed by the supervisory chip.

- If any rail connected to the config section FPGA and/or the config FPGA configuration PROM is below threshold, then the FPGA/PROM system is held in an “initialize” or reset state.

- Prior to the config FPGA being configured, the array FPGAs are held in an “initialize” or reset state.

Figure 10.2 illustrates the reset arrangement used on the Triton board.

![Figure 10.2 Triton Reset Arrangement](image-url)
11. Board Physical

The following sections provide a brief overview of the Triton board dimensions and parts placement.

11.1 Parts Placement

Figure 11.1 illustrates a parts placement for the Triton board. Overall dimensions are shown. Figure 11.2 highlights the positions of the daughter card connectors.

Figure 11.1 Triton PWB Placement and Dimensions
11.2 Daughter Card Connector Positions

Figure 11.3 illustrates the positions of the daughter cards mounted onto the Triton motherboard. This is a view from the back side of the motherboard.
Figure 11.3 Triton Daughter Card Positions
12. Chassis

A 4U-high, rack-mount chassis is being developed for the Triton motherboard. The Triton motherboard is mounted onto a steel plate, which is part of a “carrier” assembly. This carrier can be used externally to the chassis, as well as mounted inside the chassis. The carrier provides a convenient way to transport the motherboard, and allows the assembly to rest either FPGA-side up or FPGA-side down. The steel base plate provides strain relief for daughter card insertion and removal, and provides a heat-sinking path for the motherboard.

The chassis front panel provides an LCD display, a power switch, a configuration reset switch, a logic reset switch, a Compact Flash drive, and cooling fans. Apertures with cover plates are used to provide access for daughter card cables.

The following figures illustrate the chassis assembly.

Figure 12.1  Back Angle, Lid Off, FPGA Down
Figure 12.2  Back Angle, Lid Off, FPGA Up

Figure 12.3  Back Angle View, Exploded, FPGA Up
Figure 12.4  Back Angle View, Front Panel, Exploded
Figure 12.5 Back Angle View, Power Supply, Carrier

Figure 12.6 Isometric View, Exploded, FPGA Up
Figure 12.7 Isometric View, Lid On
Figure 12.8  Isometric View, Lid Off, FPGA Up
Figure 12.9 Carrier Assembly Top and Side
Figure 12.10  Carrier Assembly Bottom View