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Virtex-4 FPGA's from Xilinx

High I/O-count, 1513-pin, flip-chip BGA packages for the LX chips and 1152-pin flip-chip BGA's for the FX chips are utilized. Abundant fixed interconnects are provided between the FPGA's. All pins of all banks of each FPGA are utilized. FPGA to FPGA busses are routed and tested LVDS, run at 350MHz+ but can be used single-ended at a reduced speed. Example designs utilizing the integrated ISERDES/OSERDES with DDR for pin multiplexing are included. A 144-pin main bus (MBUS) is connected to all FPGA's, excepting the FX FPGA's, which have connectivity to 80 of these main bus signals.

Daughter cards

Nine separate 300/400-pin FCI MEG-Array connectors allow for customization with daughter cards. Signals to/from these cards are routed differentially, and can run at the limit of the FPGA: 350MHz. Clocks, resets, and presence detection, along with abundant power are included in each connector.

Memory

Four separate DDR2 SODIMM sockets are connected to FPGA's 1, 2, 13, 14. Each socket is tested to 200MHz with a DDR2 SODIMM. Standard, off-the-shelf DDR memory DIMM's (PC2-3200/PC2-4200) work nicely and we can provide these for a small charge. We have developed alternative SODIMM's that can be stuffed into these positions. Consult the factory for more details, but the list includes FLASH, SSRAM, QDR SSRAM, RLDRAM, and others.

High Speed Serial I/O Interfaces

Two FX-series chips are placed in positions 0 and 12 and can be stuffed with FX60's or FX100's. The rocketI/O's from each chip are attached to the following high-speed serial interfaces:

- 2 SFP sockets (1 MGT each)
- 2 XFP sockets (1 MGT each)
- 4 separate TX/RX via SMA's (4MGT's)
- 2 Samtec connectors for board-to-board cabling (4 MGT’s each)

Easy Configuration Via SmartMedia/Compact FLASH/USB

The configuration bit files for the FPGA's are copied onto a 128-megabyte SmartMedia or Compact FLASH card (provided) and an on-board Cypress microprocessor controls the FPGA configuration process. FPGA configuration can also be controlled via the USB interface. Visibility into the configuration process is enhanced with an RS232 port. Sanity checks are performed automatically on the configuration bit files, streamlining the configuration process. FPGA configuration occurs at the fastest possible SelectMap frequency - 48MHz. Multiple LED's provide instant status and operational feedback.

As always, reference material such as DDR SDRAM controllers, flash controllers, and PowerPC code is included (in Verilog, VHDL, C) at no additional cost.

### Virtex-4 FPGA's

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Slices (≥18k)</th>
<th>Slices or LE's</th>
<th>FF's</th>
<th>Gate Estimate</th>
<th>Max I/O's</th>
<th>FF's in I/O pad</th>
<th>Memory (18x18) Blocks</th>
<th>Memory (18x18) Total</th>
<th>Power Supply Blocks</th>
<th>Memory</th>
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<tbody>
<tr>
<td>LX100</td>
<td>90,158</td>
<td>38,204</td>
<td>1,380</td>
<td>830</td>
<td>960</td>
<td>10</td>
<td>98</td>
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<td>440</td>
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<td>32</td>
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<td>430</td>
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<td>10</td>
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<tr>
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<td>1,160</td>
<td>710</td>
<td>768</td>
<td>10</td>
<td>160</td>
<td>2</td>
<td>376</td>
<td>6,768</td>
</tr>
</tbody>
</table>

Easy Expansion via daughter cards

The DN8000K10 is easily adaptable to all applications via daughter cards. FCI Meg-Array connectors are utilized in either 300-pin or 400-pin versions and FPGA signals are routed differentially to these connectors, but can be used single-ended. Clocks and fused power are provided on each connector. Clocks can be driven from a daughter card to the global clock networks of the DN8000K10. Signals are routed from the FPGA's on a bank basis, and the daughter card selects the I/O voltage of the connector by driving the VccI/O of the FPGA bank. The I/O voltage ranges are +1.5V to +3.3V.

### Memory

<table>
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</table>
Optional 19” Rackmount Chassis

The DN8000k10 comes standard mounted to a base plate. An optional 19”, 4U-high Rackmount chassis is available. The photos below show the DN8000k10 installed in this optional chassis. The top plate is not shown.

The chassis is shipped with a Zippy Technology Corporation power supply rated at 600 watts with an AC input voltage range of 100~240 VAC. The front panel has an LCD display with an ON/OFF switch for power, and momentary switches for HARD RESET and LOGIC RESET. On the front panel connectors support the following functions:

- **MCU RS232** – FPGA configuration and control
- **USB** – Hosting and/or FPGA configuration
- **User RS232 (2,3,4)** – User RS232 ports (requires UART in FPGA)
- **Compact FLASH** – FPGA configuration

The back panel has the following connectors:

- 16 SMA’s – Directly connected to 4 Rocket I/O MGT’s
- 2 – SFP Modules
- 2 – XFP Modules