Virtex-4 Based ASIC Prototyping Engine (8-lane PCIe)

Features

- 8-lane PCI Express (PCIe) logic prototyping system available with Xilinx Virtex-4 FPGA's. Stuffing options for 1, 2, or 3 FPGA's from the following list:
  - 2 from LX family FPGA A & FPGA B (FF1513):
    - 4VLX100-10,-11,-12
    - 4VLX160-10,-11,-12
    - 4VLX200-10,-11
  - 1 from 'FX' family FPGA C (FF1152):
    - 4VFX40-10,-11,-11X,-12
    - 4VFX60-10,-11,-11X,-12
    - 4VFX100-10,-11,-11X,-12
- 100% FPGA resources available for user application
- User must supply PCIe controller
- Nearly 3.7M ASIC gates (LSI measure)
- 8-lane PCI Express (PCIe) logic prototyping
- Four, 200-pin expansion connectors with 284+ connections
- Custom daughter cards
- DN3k10SD Observation Daughter Card
- Single-ended or LVDS, +2.5/3.3V tolerant
- Full support for embedded logic analyzers via JTAG interface
- ChipScope, ChipScope PRO
- Identify™ from Synplicity
- 5 separate programmable clock synthesizers (ICS8442)
- 3 Global clocks (ACLK, BCLK, DCLK)
- PLL Clock Synthesizers
- Board Clocks
- 25 MHz
- 13 MHz
- 160 MHz
- 8442

Block Diagram
Description

The DN8000K10PCIe-8 is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN8000K10PCIe-8 is hosted in an 8-lane PCI Express slot or can be used stand-alone. The user must supply the PCIe-8 controller in FPGA A. Two Genesys Logic GL9714’s are used for the PCI Express phy function, freeing up all FX rocketI/O’s for other applications. A single DN8000K10PCIe-8 configured with 2 4VLX200’s and a single 4VFX100 can emulate up to 3.7 million gates of logic as measured by LSI. And this number does not include the embedded memories and multipliers/ALU’s resident in each FPGA. The DN8000K10PCIe-8 achieves high gate density and allows for fast target clock frequencies by utilizing FPGA’s from Xilinx’s Virtex-4 LX/FX families for logic and memory. High I/O-count, 1513-pin, flip-chip BGA packages (for LX) and 1152-pin BGA’s (for FX) are employed, providing for abundant, fixed interconnect between the FPGA’s. All FPGA interconnect is single-ended or differential, with differential clocked at 350MHz+. In addition, the OSERDES/ISERDES functionality is thoroughly tested and characterized, allowing for 10x pin multiplying on differential pairs between FPGA’s and dramatically easing the partitioning problem. Two DDR2 SDRAM SODIMM sockets are provided, allowing for up to 8GB of DDR2 memory. Each socket is tested at 200MHz, and reference designs are provided. Alternate pin-compatible SODIMMs are available that contain FLASH, RLDRAM, SSRAM, QDR SSRAM, or Mictor connectors. A total of 304+ test pins are provided on the top of the PWB via two 200-pin expansion headers. These expansion headers can also be used for logic analyzer-based debugging or for pattern generator stimulus. The DNPMC104 card can be mounted to any of these connectors, enabling an interface to A/D’s, D/A’s, and a host of other embedded system peripherals. Also, custom daughter cards can be mounted to these connectors as a means to interface the DN8000K10PCIe-8 to application-specific circuits. Two XFP modules can be used to support OC-192/STM-64, 10 Gigabit Ethernet, 10 Gigabit Fibre Channel, and G.709 data streams and can be connected to routers, switches and network cards. Reference material such as DDR2 SDRAM controllers and PowerPC code is included (in Verilog, VHDL, C) at no additional cost.

Included Accessories:

For technical applications and sales support, call 858.454.3419

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