Virtex-4 Based ASIC Prototyping Engine (1-lane PCIe)

Features
- 1-lane PCI Express logic prototyping system with up to 3 Xilinx Virtex-4 FPGA's:
  - 2 from 'LX' family FPGA A and FPGA B (FF1513):
    - 4VLX100-10, -11, -12
    - 4VLX160-10, -11, -12
    - 4VLX200-10, -11
  - 1 from 'FX' family FPGA C (FF1152):
    - 4VLX200-10, -11, -12
- All FPGA to FPGA interconnect LVDS differential
- 350MHz differential chip to chip
- Reference designs for integrated ISERDES/OSERDES
  - 10x pin multiplexing per LVDS pair
  - FPGA A to FPGA B interconnect: >1800 signals
  - Greatly simplified logic partitioning
  - Synplicity Certify™ models for partitioning assistance
- 5 separate programmable clock synthesizers (ICS8442)
  - 3 Global clocks (ACLK, BCLK, DCLK)
  - 2 for RocketI/O specific functions
  - User configurable via SmartMedia, PCI, or USB
- Gigabit serial I/O interfaces:
  - 2 -- 10G, Small form factor XFP (or SFP) modules
  - SMA connectors for off-board cabling of 4 channels of RocketI/O
- Clocking options available for standard communications data rates for RocketIO:
  - 10Gbps
  - Samtec cables for off-board cabling of 10 channels of RocketI/O (~4Gbps)
  - Clocking options available for standard communications data rates for RocketIO:
  - OIF 10G BP, 10G Ethernet, OC-192, OC-12, Aurora
- 1x, 2x, 4x Fibre Channel, 10G Fibre Channel

Block Diagram

[Diagram showing the connectivity and components within the Virtex-4 Based ASIC Prototyping Engine, including FPGA configurations, clocking options, and interfaces such as PCIe, DDR2 SODIMM, and JTAG.]
Description

The DN8000K10PCIe is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN8000K10PCIe is hosted in a 1-lane PCI Express slot or can be used stand-alone. The user must supply the PCIe controller in FPGA A. The NXP PX1011A performs the PCI Express Phy function, freeing up all FX rocketI/O's for other applications. A single DN8000K10PCIe configured with 2 4VLX200's and a single 4VFX100 can emulate up to 3.7 million gates of logic as measured by LSI. And this number does not include the embedded memories and multipliers/ALU's resident in each FPGA. The DN8000K10PCIe achieves high gate density and allows for fast target clock frequencies by utilizing FPGA's from Xilinx's Virtex-4 LX/FX families for logic and memory. High I/O-count, 1513-pin, flip-chip BGA packages (for LX) and 1152-pin BGA's (for FX) are employed, providing for abundant, fixed interconnect between the FPGA's. All FPGA interconnect is single-ended or differential, with differential clocked at 350MHz+. In addition, the OSERDES/ISERDES functionality is thoroughly tested and characterized, allowing for 10x pin multiplying on differential pairs between FPGA's and dramatically easing the partitioning problem. Two DDR2 SDRAM SODIMM sockets are provided, allowing for up to 8GB of DDR2 memory. Each socket is tested at 200MHz, and reference designs are provided. Alternate pin-compatible SODIMMs are available that contain FLASH, RLDRAM, SSRAM, QDR SSRAM, or Mictor connectors. A total of 304+ test pins are provided on the top of the PWB via two 200-pin expansion headers. These expansion headers can also be used for logic analyzer-based debugging or for pattern generator stimulus. The DNPMC104 card can be mounted to any of these connectors, enabling an interface to A/D's, D/A's, and a host of other embedded system peripherals. Also, custom daughter cards can be mounted to these connectors as a means to interface the DN8000K10PCIe to application-specific circuits. Two XFP modules can be used to support OC-192/STM-64, 10 Gigabit Ethernet, 10 Gigabit Fibre Channel, and G.709 data streams and can be connected to routers, switches and network cards. Reference material such as DDR2 SDRAM controllers and PowerPC code is included (in Verilog, VHDL, C) at no additional cost.

For technical applications and sales support, call 858.454.3419