1) FPGA design cannot meet timing when using the QL5064_module_interface module provided by the Dini Group.

Due to a design error, the signal used for clocking the PCI interface from FPGA A to the QL5064 PCI bridge chip (CLKP) is connected to a non-global clock pin on FPGA A. As a result, the clock signal inside the FPGA is skewed by a large, non-consistent time delay. This makes it very hard to meet timing in the FPGA using the provided module.

Affected Customers

Customers with revision 1 boards shipped before October 20, 2006 who need to use DMA communication over PCI to FPGA A are affected. When using PCI to communicate over Main Bus this issue does not apply. When using target accesses to BAR0 through BAR7, it is possible to run the QL5064_interface_module module without meeting timing, since the interface is a multi-cycle path.

Resolution

The current suggested resolution to this problem is to rework the board to connect this signal to a global clock pin. The Dini Group will perform this rework. The rework involves adding two wires to the back side of the PCB. Dini Group does not recommend performing the rework yourself. After the rework is performed, the pin AH19 will be used on FPGA A as the CLKP input.