The DN9000k10 is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN9000k10 is stand-alone or hosted via a USB interface. A single DN9000k10 configured with 16 Xilinx Virtex-5, XC5VLX330’s can emulate up to 32 million gates of logic as measured by LSI. This number does not include the embedded memories and multipliers resident in each FPGA. The DN9000k10 achieves high gate density and allows for fast target clock frequencies by utilizing FPGA’s from Xilinx’s Virtex-5 FPGA family for logic and memory. All FPGA resources are available for the target application. Any subset of FPGA’s can be stuffed.

### Features

- **USB2.0-hosted logic prototyping system with 2-16 Xilinx Virtex-5 FPGA’s**
  - 16 LX330’s (FFI760):
    - 100% FPGA resources available for user application
  - 32M+ ASIC gates (LSI measure) with 16 LX330’s
  - FPGA to FPGA interconnect is single-ended or LVDS
    - 450Mhz differential chip-to-chip DDR (900Mb/s)
    - Reference designs for integrated I/O pad ISERDES/OSERDES
    - 10x pin multiplexing per LVDS pair
    - Greatly simplified logic partitioning
    - Source synchronous clocking for LVDS
  - Main Busses for global connectivity:
    - Main Bus Horizontal (MBH), all FPGAs: 80 single-ended signals
    - Main Bus Vertical (MBV), right two columns of FPGAs: 80 single-ended signals
  - Auspy AES models for partitioning assistance
    - And hooks for other third-party partitioning solutions
  - 6 separate DDR2 SODIMMs (250MHz)
    - 64-bit data width, 250MHz operation
    - PC2-5300
    - Addressing/power to support 4GB in each socket
    - DDR2 Verilog/VHDL reference design provided (no charge)
    - DDR2 SODIMM data transfer rate: 32GB/s
    - Alternate pin compatible memory cards available:
      - QDR SSRAM, Micror, RLDRAM, SSRAM, DDR3, interconnect, SDRAM DRAM, FLASH, and others
  - 3 board-level global clock networks (GCLK0, GCLK1, GCLK2)
    - Separate programmable synthesizers for each network
    - User configurable via Compact FLASH or USB
    - Separate global reference clock network for IDELAY chain delay resolution (REFCLK)
    - Global clocks networks distributed differentially and balanced
    - Single-step clocking available on each global clock network
    - 3 external differential clock inputs can be multiplexed in to global clock networks (via SMA’s)
    - 8, 400-pin MEG-Array connectors (FCI)
      - 96 LVDS pairs + clocks (or 192 single-ended)
      - 450MHz on all signals with LVDS
      - Reset, presence detect
      - Supplied power rails (fused):
        - +12V (24W max)
        - +5V (10W max)
        - +3.3V (10W max)
      - Pin multiplexing to/from daughter cards using ISERDES/OSERDES and LVDS (up to 10x)
  - Fast and Painless FPGA configuration
    - Compact FLASH, and/or USB
    - Fast and painless configuration readback
    - 4 separate parallel readback busses
  - Custom base plate (standard) and optional rackmount chassis
  - Protection from those drooling engineers
  - 4, RS232 ports for PowerPC or embedded uP debug
    - Accessible from all FPGA’s via Configuration FPGA
  - Full support for embedded logic analyzers via JTAG interface
    - ChipScope, ChipScope Pro and other third party tools
  - Convert a pair of MEG-Array expansion connectors to interconnect with the DNMEG_Intercon
    - Add 186 single-ended OR 93 pairs LVDS:
      - (FPGA 8 to 12)
      - (FPGA 3 to 7) AND/OR (FPGA 11 to 15)
  - Enough status LED’s to perform a cosmetic peel on the face of a walrus

### Description

**Overview**

The DN9000k10 is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN9000k10 is stand-alone or hosted via a USB interface. A single DN9000k10 configured with 16 Xilinx Virtex-5, XC5VLX330’s can emulate up to 32 million gates of logic as measured by LSI. This number does not include the embedded memories and multipliers resident in each FPGA. The DN9000k10 achieves high gate density and allows for fast target clock frequencies by utilizing FPGA’s from Xilinx's Virtex-5 FPGA family for logic and memory. All FPGA resources are available for the target application. Any subset of FPGA’s can be stuffed.
Virtex-5 FPGA’s from Xilinx
High I/O-count, 1760-pin, flip-chip BGA packages are utilized. Abundant fixed interconnects are provided between the FPGA’s. All pins of all banks of each FPGA are utilized. FPGA to FPGA busses are routed and tested LVDS, run at 450MHz+ but can be used single-ended at a reduced speed. Example designs utilizing the integrated ISERDES/OSERDES with DDR for pin multiplexing are included. An 80-pin main bus horizontal (MBH) is connected to all FPGA’s and another 80-pin Main Bus vertical (MBV) is connected to the 8 FPGA’s in the right two columns.

Daughter Cards
Eight separate 400-pin FCI MEG-Array connectors allow for customization with daughter cards. Signals to/from these cards are routed differentially, and can run at the limit of the FPGA: 450MHz. Clocks, resets, and presence detection, along with abundant power are included in each connector. The DNMEG_Intercon card van be used to convert any, or all, of these connectors to interconnect.

Memory
Six separate DDR2 SODIMM sockets are connected to FPGA’s 0-2, 12-14. Each socket is tested to 250MHz with a DDR2 SODIMM. Standard, off-the-shelf DDR2 memory DIMM’s (PC2-5300) work nicely and we can provide these for a small charge. We have developed alternative SODIMM’s that can be stuffed into these positions. Consult the factory for more details, but the list includes FLASH, SSRAM, QDR SSRAM, RLDRAM, SDR SDRAM, mictors and others.

Easy Configuration Via Compact FLASH or USB
The configuration bit files for the FPGA’s are copied onto a 128-megabyte Compact FLASH card (provided) and an on-board Cypress microprocessor controls the FPGA configuration process. FPGA configuration can also be controlled via the USB interface. Fully stuffed, the DN9000k10 configures in less than 60 seconds. Visibility into the configuration process is enhanced with an RS232 port. Sanity checks are performed automatically on the configuration bit files, streamlining the configuration process. FPGA configuration occurs at the fastest possible SelectMap frequency - 48MHz. Multiple LED’s provide instant status and operational feedback. Laboratory testing is showing that the amount of illumination provided by the LED’s is enough to perform sophisticated cosmetic procedures on a walrus. As always, reference material such as DDR2 SDRAM controllers, flash controllers, et al. is included (in Verilog, VHDL, C) at no additional cost.

Easy Expansion via Daughter Cards
The DN9000k10 is easily adaptable to all applications via daughter cards. FCI Meg-Array connectors are utilized in the 400-pin version and FPGA signals are routed differentially to these connectors, but can be used single-ended. Clocks and fused power are provided on each connector. Clocks can be driven from a daughter card to the global clock networks of the DN9000k10. Signals are routed from the FPGA’s on a bank basis, and the daughter card selects the I/O voltage of the connector by driving the VccI/O of the FPGA bank. The I/O voltage ranges are +1.5V to +3.3V.

Optional 19” Rackmount Chassis
The DN9000k10 comes standard mounted to a base plate. An optional 19”, 4U-high Rackmount chassis is available. The photos on the following pages show the DN9000k10 installed in this optional chassis. The top plate is not shown. The chassis is shipped with a Zippy Technology Corporation power supply rated at 600 watts with an AC input voltage range of 100~240 VAC. The front panel has an LCD display with an ON/OFF switch for power, and momentary switches for HARD RESET and LOGIC RESET. On the front panel connectors support the following functions:

- **MCU RS232** – FPGA configuration and control
- **USB** – Hosting and/or FPGA configuration
- **User RS232 (2,3,4)** – User RS232 ports (requires UART in FPGA)
Block Diagram

- = LVDS when paired, but can be run single-ended at reduced frequency
Photos
Included Accessories:

For technical applications and sales support, call 858.454.3419

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