Features

- PCI Express (8-lane) logic prototyping system with 2-6 Xilinx Virtex-5 FPGA’s
  - XC5VLX330-1, -2 (FF1760)
- Xilinx Virtex-5T for PCIe interface and controller
  - PCIe GEN1 rev 1.1 with LX50T (8-lanes)
  - PCIe GEN2 (4-lanes)
- 100% FPGA interconnect is single-ended or LVDS
- Nearly 12M ASIC gates (LSI measure) with 6 Virtex-5 LX330’s
- FPGA to FPGA interconnect is single-ended or LVDS
  - 450Mhz LVDS chip to chip (900 MB/s)
  - Slightly slower when used single-ended (~225MHz)
- Reference designs for integrated I/O pad
- 1 SODIMM for FPGA and DDR2 SODIMMs (250MHz)
- Auspy models for partitioning assistance
- 6 separate DDR2 SODIMMs (250MHz)
  - 1 SODIMM for FPGA’s A, B, F, D
  - 2 SODIMM’s for FPGA C
- Eight independent low-skew global clock networks
  - G0, G1, G2, M4, EXT0, EXT1, FBB, FB, REF250
- Three, high-resolution, user-programmable synthesizers for G0, G1, G2
- User configurable via CompactFlash, USB, PCIe, JTAG
- Global clocks networks distributed differentially and balanced
- Three independent single-step clocks
- Up to three independent external clocks inputs (single-ended or differential) can be injected onto low-skew global clock networks

Description

Overview

The DN9000k10PCIe-8T is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype PCIe-based logic and memory designs for a fraction of the cost of existing solutions. The DN9000k10PCIe-8T is hosted in an 8-lane PCIe bus, but can be used stand-alone and configured via USB and/or CompactFlash. A single DN9000k10PCIe-8T configured with 6 Xilinx Virtex-5, XC5VLX330’s can emulate up to 12 million gates of logic as measured by LSI (or at least how LSI used to measure ASIC gates when they manufactured ASIC’s). This number does not include the embedded memories and multipliers resident in each FPGA, all of which are 100% available to the user application. The DN9000k10PCIe-8T achieves high gate density and allows for fast target clock frequencies by utilizing the largest FPGA from Xilinx’s Virtex-5 FPGA family for logic and memory. All FPGA resources are available for the target application. Any subset of FPGA’s can be stuffed along with any combination of speed grades.

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Speed Grades</th>
<th>Slices or LE's</th>
<th>FF's</th>
<th>Gate Estimate</th>
<th>Multipliers (kBytes)</th>
<th>Memory</th>
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<td>Max (1000)</td>
<td>Max (1000)</td>
<td>Blocks</td>
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<td>Total</td>
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<td></td>
<td></td>
<td></td>
<td>(1000)</td>
<td>(1000)</td>
<td>Total</td>
</tr>
<tr>
<td>Virtex-5</td>
<td></td>
<td></td>
<td></td>
<td>(1000)</td>
<td>(1000)</td>
<td></td>
</tr>
<tr>
<td>LX330</td>
<td>-1, -2</td>
<td>51,840</td>
<td>207,360</td>
<td>3,320</td>
<td>1,990</td>
<td>192</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1,200</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Virtex5T</td>
<td></td>
<td></td>
<td></td>
<td>(1000)</td>
<td>(1000)</td>
<td>Blocks</td>
</tr>
<tr>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td>(1000)</td>
<td>(1000)</td>
<td></td>
</tr>
<tr>
<td>FX70T</td>
<td>-1, -2, -3</td>
<td>11,200</td>
<td>48,640</td>
<td>778</td>
<td>467</td>
<td>128</td>
</tr>
<tr>
<td>SX50T</td>
<td>-1, -2, -3</td>
<td>8,160</td>
<td>32,640</td>
<td>520</td>
<td>312</td>
<td>100</td>
</tr>
<tr>
<td>LX50T</td>
<td>-1, -2, -3</td>
<td>7,200</td>
<td>28,800</td>
<td>460</td>
<td>276</td>
<td>100</td>
</tr>
<tr>
<td>SX35T</td>
<td>-1, -2, -3</td>
<td>5,440</td>
<td>21,760</td>
<td>350</td>
<td>210</td>
<td>100</td>
</tr>
<tr>
<td>FX30T</td>
<td>-1, -2, -3</td>
<td>5,120</td>
<td>20,480</td>
<td>328</td>
<td>197</td>
<td>100</td>
</tr>
<tr>
<td>LX30T</td>
<td>-1, -2, -3</td>
<td>4,800</td>
<td>19,200</td>
<td>310</td>
<td>186</td>
<td>100</td>
</tr>
</tbody>
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The DN9000K10PCIe-8T is a Xilinx Virtex-5 Based ASIC Prototyping Engine 8-lane PCI Express (Virtex-5T)
Block Diagram

- **FPGA A**: Virtex 5, LX330 (FF1760)
- **FPGA B**: Virtex 5, LX330 (FF1760)
- **FPGA C**: Virtex 5, LX330 (FF1760)
- **FPGA D**: Virtex 5 LX330 (FF1760)
- **FPGA E**: Virtex 5 LX330 (FF1760)
- **FPGA F**: Virtex 5 LX330 (FF1760)

**Clock Sources**:
- GCLK0, GCLK1, GCLK2
- EXT0, EXT1 (zero delay)
- MB48CLK48MHz
- PLL(FF1760)

**Data Interfaces**:
- PCIe Express 8-lane
- 10 GE (VSC8201)
- RS232
- SPI FLASH 16Mb
- DDR2 SODIMM (4GB Max)
- Compact FLASH

**Connecting Features**:
- SMA connectors
- JTAG
- PLL
- MICTOR

**Additional Components**:
- Alternate SODIMMs: SSRAM, DDR3, FLASH, Test Points, DRAM, USB PHY, RLDRAM (ALL DDR2 Sockets)
- LVDS when paired, but can be used single-ended at reduced frequency

**Board Specifications**:
- 8-lane PCIe Express ASIC Prototyping Board with Virtex-5 FPGAs
- Virtex-5 FPGAs
- USB 2.0 (480 Mb/s)
- RS232
- Compact FLASH Configuration

The DINI group
Dedicated Virtex-5T FPGA for PCIe, 8-lane controller
A Xilinx Virtex-5 LX50T FPGA is used to host the PCI Express controller. We ship a full function, fixed, 8-lane master/target with the product, along with drivers and ‘C’ source for several operating systems. The user can use this FPGA for emulating his/her own controller or third-party IP. GEN2 PCIe (4-lanes) is handled with an FXT70 stuffing option.

Virtex-5 FPGAs from Xilinx
The DN9000k10PCIe-8T uses high I/O-count, 1760-pin, flip-chip BGA packages. Abundant fixed interconnects (either differential or single-ended) are provided between the FPGA’s. All pins of all banks of both FPGA are utilized. FPGA to FPGA busses are routed and tested LVDS, run at 450MHz+ (which is 900 Mb/s if used in DDR mode). Single-ended at the reduced speed of 225MHz is characterized and tested. Example designs utilizing the integrated ISERDES/OSERDES with DDR for pin multiplexing are included. A 164-pin main bus (MB) is connected to all FPGAs including the Spartan configuration FPGA, allowing for data movement via USB.

Daughter cards
Three separate 400-pin FCI MEG-Array connectors allow for customization with daughter cards. Signals to/from these cards are routed differentially and can run at the limit of the FPGA: 450MHz. Clocks, resets, and presence detection, along with abundant power are included in each connector. Two adjacent MEG-Array connectors can be converted to FPGA to FPGA interconnect with a DNMEG_Intercon.

Memory
Six separate DDR2 SODIMM sockets are stuffed and have connections to FPGA’s A, B, D, F, and C (two separate sets). Each socket is tested to 250MHz with a DDR2 SODIMM. Standard, off-the-shelf DDR2 memory DIMM’s (PC2-4200 or better) work nicely and we can provide these for a small charge. We have developed alternative SODIMM’s that can be stuffed into these positions. Consult the factory for more details, but the list includes FLASH, SSRAM, QDR SSRAM, mictors, USB PHYs, DDR3, and others.

Easy Configuration Via Compact FLASH, PCIe or USB
The configuration bit files for the FPGA's are copied onto a Compact FLASH card (provided) and an on-board Cypress microprocessor controls the FPGA configuration process. FPGA configuration can also be controlled via the USB interface or downloaded via PCIe. Visibility into the configuration process is enhanced with an RS232 port. Sanity checks are performed automatically on the configuration bit files, streamlining the configuration process. FPGA configuration occurs at the SelectMap frequency - 48MHz. Multiple LED's provide instant status and operational feedback. As always, reference material such as a DDR2 SDRAM controller is included (in Verilog, VHDL) at no additional cost.

Status LED’s, Debug
Although no animal testing was performed, sophisticated statistical models are showing that the 90 status LED’s is enough to disturb the circadian cycle of an elderly Sun fish (DCCSF). Please don’t try this at home – the fish tend to get quite testy when their sleep cycles are altered. These LED’s are user controllable from the FPGA’s so can be used as visual feedback in addition to irritating large, bizarre fish. A JTAG connector provides an interface to Chipscope and other third party debug tools. Other FPGA debug solutions will be available later in ‘07.