The DN9002k10PCI is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN9002k10PCI is hosted on a 32/64-bit, 33/66MHz PCI bus, or can be used stand-alone and configured via USB or Compact FLASH. A single DN9002k10PCI stuffed with 2 Xilinx Virtex-5, XC5VLX330’s can emulate up to 4 million gates of logic as measured by LSI (or at least how LSI used to measure ASIC gates when they manufactured ASIC’s). This number does not include the embedded memories and multipliers resident in each FPGA, all of which are 100% available to user application. The DN9002k10PCI achieves high gate density and allows for fast target clock frequencies by utilizing FPGA’s from Xilinx's Virtex-5 FPGA family for logic and memory. All FPGA resources are available for the target application. Any subset of FPGA’s can be stuffed.

### Features

- **PCI-hosted logic prototyping system with 1-2 Xilinx Virtex-5 FPGA’s in FF1760 package** (slowest to fastest):
  - XC5VLX110-1,-2,-3
  - XC5VLX220-1,-2
  - XC5VLX330-1,-2
- **100% FPGA resources available for user application**
- **Nearly 4M ASIC gates (LSI measure) with 2 LX330’s**
- **FPGA to FPGA interconnect is single-ended or LVDS**
  - 450Mhz DDR LVDS (900Mb/s) chip to chip, or 225 MHz single-ended
  - Reference designs for integrated I/O pad
  - ISERDES/OSERDES
  - 10x pin multiplexing per LVDS pair
  - Greatly simplified logic partitioning
  - Source synchronous clocking for LVDS
- **Main Bus (MB) – 40 signals**
  - Single-ended
  - Connects to both FPGAs and Config FPGA
- **Auspy models to aid automatic partitioning**
- **DDR2 SODIMM (200MHz) on FPGA B**
  - 64-bit data width, 200MHz operation
  - PC2-3200/PC2-4200
  - Addressing/power to support 4GB in each socket
  - DDR2 Verilog/VHDL reference design provided (no charge)
  - DDR2 SODIMM data transfer rate: 25.6Gb/s
  - Alternate pin compatible memory cards available (consult factory for availability):
    - QDR SDRAM, FLASH, SDRAM,
    - RLDRAM, Micror, DDR1, DDR3
- **3 board-level global clock networks (GCLK0, GCLK1, GCLK2)**
  - Separate programmable synthesizers for each network
  - User configurable via Compact Flash or USB
  - Global clocks networks distributed differentially and balanced
  - Single-step clocking available on each global clock network
- **Flexible customization via daughter cards**
  - 2, 400-pin Meg-Array connectors (FCI)

### Description

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### Used in Model

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Speed Grades (slowest to fastest)</th>
<th>Slices or LE’s</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Max I/O’s</th>
<th>FF’s in I/O</th>
<th>Multipliers (2x18)</th>
<th>Used in Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex5</td>
<td></td>
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Virtex-5 FPGA’s from Xilinx

The DN9002k10 uses high I/O-count, 1760-pin, flip-chip BGA packages. Abundant fixed interconnects (either differential or single-ended) are provided between the FPGA’s. All pins of all banks of both FPGA are utilized. FPGA to FPGA busses are routed and tested LVDS, run source synchronously at 450MHz+ but can be used single-ended at a reduced speed. Example designs utilizing the integrated ISERDES/OSERDES with DDR for pin multiplexing are included. A 36-pin main bus (MB) is connected to both FPGA’s including the Spartan configuration FPGA, allowing for data movement via USB.

Daughter Cards

Two separate 400-pin FCI MEG-Array connectors allow for customization with daughter cards. Signals to/from these cards are routed differentially, and can run at the limit of the FPGA: 450MHz. Clocks, resets, and presence detection, along with abundant power are included in each connector.

Memory

A single DDR2 SODIMM socket is stuffed and is connected to FPGA B. The socket is tested to 250MHz with a DDR2 SODIMM. Standard, off-the-shelf DDR2 memory DIMM’s (PC2-3200/PC2-4200) work nicely and we can provide these for a small charge. We have developed alternative SODIMM’s that can be stuffed into these positions. Consult the factory for more details, but the list includes FLASH, SSRAM, QDR SSRAM, mictors, DDR1, and others.

Easy Configuration Via Compact FLASH or USB

The configuration bit files for the FPGA's are copied onto a Compact FLASH card (provided) and an on-board Cypress microprocessor controls the FPGA configuration process. FPGA configuration can also be controlled via the USB interface. Visibility into the configuration process is enhanced with an RS232 port. Sanity checks are performed automatically on the configuration bit files, streamlining the configuration process. FPGA configuration occurs at the fastest possible SelectMap frequency - 48MHz. Multiple LED’s provide instant status and operational feedback.

Other Cool Stuff

Many FPGA-controlled LEDs provide for visual status. Although no laboratory testing was performed, statistical animal models are showing this to be enough illumination to blind four very rare, endangered, slightly confused Pacific Northwest tree octopi (Octopus paxarbolis) A Mictor connector, which has 34 FPGA signals, enables observation via logic analyzers from Tektronix and HP.
Included Accessories: