Features

- Hosted in a 4-lane GEN1 PCIe slot or stand-alone
  - 4-lane GEN1 PCIe (v1.1) slot
  - USB 2.0
  - 10/100/1000 baseT Ethernet
- Stand-alone
- 1-2 Xilinx Virtex-6 FPGAs from the following list:
  - SX475T-2,-1,-1L (fastest to slowest)
  - SX315T-3,-2,-1,-1L
  - LX365T-3,-2,-1,-1L
  - LX240T-3,-2,-1,-1L
  - LX195T-3,-2,-1,-1L
  - LX130T-3,-2,-1,-1L
- 50A $V_{CCINT}$ power shared between both FPGAs
- FF1156 package with 600 I/Os, all utilized
- 10+ million ASIC gates (ASIC measure) when
  stuffed with 2 Virtex-6 SX475T
- 2016, 25 x 18 multipliers (with accumulator)
- per SX475
- FPGA to FPGA interconnect is LVDS
  - 710 MHz LVDS chip to chip with -3 speed grade
  - 500 MHz with -2 (1.0 Gb/s with DDR)
  - 650 MHz with -1 (1.3 Gb/s with DDR)
- Pairs are length balanced and tested!
- LVDS pairs can be used as two single-ended
  signals at reduced frequency (~225MHz)
- Reference designs for integrated I/O pad
  ISERDES/OSERDES
- 10x pin multiplexing per LVDS pair
- Greatly simplified logic partitioning
- Source synchronous clocking for LVDS
- RocketIO GTX Transceivers
  - 6.5 Gb/s (with -3, -2 speed grade)
  - 5.0 Gb/s with -1
  - 4-lanes connected from FPGA A and FPGA B
  - 2 lanes connected from Config FPGA Q to FPGA A
  - 2 lanes connected from Config FPGA Q to FPGA B
- Data examples provided using Aurora protocol
- Auspy models for logic partitioning assistance
- Marvell MV78200 Discovery Innovation Dual CPU
  - 1 GHz clock
  - Dual USB 2.0 ports (Type B connector)
  - Dual Serial-ATA II (SATA)
  - Gigabit Ethernet interface
  - 10/100/1000 GbE (RJ45 connector)

ASIC Prototyping Engine Featuring Xilinx Virtex-6
Hosted via 4-lane PCI Express (GEN1)

### Memory

<table>
<thead>
<tr>
<th>LUT Size</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Multiplicers (2x18)</th>
<th>Blocks (18kbits)</th>
<th>Total (kbits)</th>
<th>Total (kbytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Max (100% util)</td>
<td>Practical (60% util)</td>
<td>Max I/O’s</td>
<td>180's</td>
<td>25%</td>
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</table>

### Virtex-6

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Speed Grades (slowest to fastest)</th>
<th>LUT Size</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Multiplicers (2x18)</th>
<th>Blocks (18kbits)</th>
<th>Total (kbits)</th>
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</thead>
<tbody>
<tr>
<td>SXT</td>
<td>-1L,-1,-2</td>
<td>6-input</td>
<td>595200</td>
<td>5,714</td>
<td>3,428</td>
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<td>SX315T</td>
<td>-1L,-1,-2,-3</td>
<td>6-input</td>
<td>394000</td>
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<td>2,269</td>
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<td>-1L,-1,-2,-3</td>
<td>6-input</td>
<td>301440</td>
<td>2,894</td>
<td>1,726</td>
<td>600</td>
<td>768</td>
<td>832</td>
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<tr>
<td>LX240T</td>
<td>-1L,-1,-2,-3</td>
<td>6-input</td>
<td>249900</td>
<td>2,396</td>
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<td>600</td>
<td>640</td>
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<td>LX195T</td>
<td>-1L,-1,-2,-3</td>
<td>6-input</td>
<td>160300</td>
<td>1,536</td>
<td>922</td>
<td>600</td>
<td>480</td>
<td>528</td>
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<tr>
<td>LX130T</td>
<td>-1L,-1,-2,-3</td>
<td>6-input</td>
<td>160000</td>
<td>1,536</td>
<td>922</td>
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</tbody>
</table>
Description

Overview

The **DN-DualV6-PCIe-4** is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The **DN-DualV6-PCIe-4** is hosted in a 4-lane PCIe bus (GEN1), but can be used stand-alone and configured via USB or Ethernet. A single **DN-DualV6-PCIe-4** configured with 2 Xilinx Virtex-6, SX475Ts can emulate up to 10 million gates of logic as measured by a reasonable ASIC gate counting standard. This gate count estimate number does not include embedded memories and multipliers resident in each FPGA. Note that the SX475 has 2,016 25x18 multipliers per FPGA. One hundred percent (100%) of the Virtex-6 FPGA resources are available to the user application. The **DN-DualV6-PCIe-4** achieves high gate density and allows for fast target clock frequencies by utilizing FPGAs from Xilinx’s 40nm Virtex-6 family. You can mix and match FPGAs. Any subset of FPGAs can be stuffed and we can accommodate any combination of speed grades in the two FPGA positions.

Virtex-6 FPGAs from Xilinx

The **DN-DualV6-PCIe-4** uses high I/O-count, 1156-pin, flip-chip BGA packages. This package has 600 I/Os and all are utilized. Abundant fixed interconnects (either differential or single-ended) are provided between the FPGAs. FPGA to FPGA buses are routed and tested LVDS and run at 710 MHz+ (which is 1.4 Gb/s when used in DDR mode and assumes a -3 speed grade FPGA). Single-ended at the reduced speed of 225MHz is characterized and tested. Example designs utilizing the integrated I/O shift registers (ISERDES/OSERDES) with DDR for pin multiplexing are included. Two 20-pair LVDS busses connect FPGAs A and B to the configuration FPGA (**Config FPGA Q**). The connection to the **Config FPGA Q** allows for data movement via USB/PCIe/Ethernet/SATA/et. al. to any/all FPGAs. The FPGAs share a 50A VCCINT power supply.

Six possible Virtex-6 FPGAs can be stuffed in the A and B positions. You are free to mix and match any FPGA and any available speed grade from the following list (fastest to slowest): **SX475T-2,-1,-1L**, **SX315T-3,-2,-1,-1L**, **LX365T-3,-2,-1,1L**, **LX240T-3,-2,-1,1L**, **LX195T-3,-2,-1,1L**, **LX130T-3,-2,-1,1L**.

The Marvell MV78200 Discovery™ Dual CPU

A **MONSTER** for data movement and manipulation

Easy FPGA configuration is a required feature of large, multi-FPGA boards. We use an onboard CPU to handle this function. We choose a Marvell MV78200 from the Discovery™ Innovation CPU family. Bluntly stated, this CPU is massive overkill for the mundane task of FPGA configuration. The MV78200 has a variety high performance interfaces and features, and all can be utilized to your advantage.
**Dual Sheeva™ CPUs, 1GHz with floating point**

First and foremost are dual CPUs. And after we are done configuring the FPGAs we dedicate both CPUs to your application. The CPUs in the MV78200 are Marvell Sheeva™ cores, which are ARM v5TE compliant. The CPUs are clocked at 1GHz and each processor has a single and double precision floating point unit. A fixed 1 GB, DDR2 memory is standard and is useful for large amounts of high speed data buffering. The memory is organized as 128M x 64 and clocked at the full frequency allowed: 400MHz (800 MHz effective with DDR). This DDR2 bank is shared between the two CPUs. Boot code is resident in an SPI FLASH, and application code is downloaded via any port: PCIe, USB, and Ethernet. We ship LINUX as the standard operating system. Options exist for VxWorks and other real-time operating systems. Contact the factory for more information.

**PCI Express**

The Marvell 78200 has two 4-lane GEN1 PCIe ports (2.5 GHz). The first, PORT0, is connected to the fingers on the circuit board and is used as the default approach to hosting the DN-DualV6-PCIe-4. Full master mode is supported and multiple DMA engines ease the task of high speed data movement to/from any port. Multiple DN-DualV6-PCIe-4s can be placed in a single backplane, but be aware that this product may take two slots due to the heat sinks required. The second 4-lane PCIe port, PORT1, is connected FPGA-Q (Virtex-5 LX50T-2). We ship a full PCIe bridge in FPGA-Q, enabling data movement between the MV78200 and FPGA-Q at the fastest performance 4-lanes of GEN1 PCIe allows. Note that the MV78200 is a non-transparent PCIe bridge, so some driver support in the MV78200 is necessary. We, of course, supply these drivers for no cost.

Two Serial-ATA Ports (SATA II)
The MV78200 has two Serial-ATA Generation 2i ports (SATA II), each capable of running at 3.0 Gb/s. SATA is intended for high speed data transfer to/from a hard drive. Connectors are provided for both of these SATA ports, enabling a direct connection to external hard drives. Both FPGA A and FPGA B have dual SATA connectors connected to rocketI/O MGTs. With SATA IP integrated into the FPGA logic, SATA cables connected can provide additional high-speed data paths between the field FPGAs and the Marvell processors. Note that the MV78200 has specialized enhanced DMA (EDMA) engines for SATA and a dedicated 512-byte buffer for each channel. The EDMA features are too numerous to detail here but, these high speed SATA ports can be used to transfer data to any port of the MV78200. The partial list includes FPGA A – FPGA B, FPGA A/B – USB, FPGA A/B – PCIe, FPGA A/B – Ethernet, FPGA A/B – Memory, and others. Examples of all possible options, with source, are included, but FPGA SATA IP is not included.

GbE – 802.3 Gigabit Ethernet

The MV78200 has 4 GbE ports. We use one.

**Daughter cards**

A 400-pin FCI MEG-Array connector is directly attached to FPGA B, allowing for customization with daughter cards. This is a non-proprietary industry standard connector family and the mating connector is readily available. We can provide them to you at our cost. We are not fans of proprietary, outrageously priced connectors. The 198 signals to and from this card are routed differentially and can run at the limit of the FPGA I/Os: 710 MHz (assumes a -3 speed grade). Clocks, resets, and presence detection, along with abundant (fused) power are included in each connector.

**Memory**

Two separate DDR3 SODIMM sockets are connected to each Virtex-6 FPGA. This style of SODIMM is 64-bits. Each socket is tested to 533MHz with a PC3-8500 DDR3 SODIMM. Standard, off-the-shelf DDR3 memory SODIMMs work fine and we can provide these for a small charge. The maximum memory size is probably 4GB in the short term. We have developed alternative SODIMM’s that can be stuffed into these positions. Consult the factory for more details, but the list includes FLASH, SSRAM, QDR SSRAM, mictors, USB PHYs, DDR2, RLDRAM, and others. As always, reference material such as a DDR3 SDRAM controller is included (in Verilog, VHDL) at no additional cost.

**Easy Configuration via PCIe, USB, or Ethernet**

If the DN-DualV6-PCIe-4 is hosted via PCIe, USB, or Ethernet, FPGA configuration occurs via the host under the control of one of the Marvell CPUs. If the board is used standalone, the FPGA configuration files are copied onto a USB stick and FPGA configuration occurs at power up after the Marvell processors have booted (~15 seconds). Sanity checks are performed automatically on the configuration bit files, streamlining the configuration process in the case of errors. Multiple LEDs provide instant status and operational feedback.
Status LEDs, Debug
Although no specific testing was performed, sophisticated statistical finite element models and back of the envelope calculations are showing the dozens of status LEDs to be bright enough to be seen from a low earth orbit. Please don’t try this at home since the risk is high and the dangers great. When testing this feature, make sure an adult is present. These LEDs are user controllable from the FPGAs so can be used as visual feedback in addition to illumination. A JTAG connector provides an interface to ChipScope and other third party debug tools.