Features

• PCI Express (4-lane) FPGA-based algorithm acceleration peripheral with 5 Kintex-7 FPGAs
  - 4 Xilinx Kintex-7 FPGAs (FFG676)
    • 7K410T-3,-2,-1, 7K325T-3,-2,-1, or 7K160T-3,-2,-1
  - 1 Xilinx Kintex-7 FPGA (FFG900)
    • 7K410T-3,-2,-1 or 7K325T-3,-2,-1
• Fixed 4-lane PCIe interface and controller
  - PCIe GEN1/GEN2
  - Full mastering DMA
    • 2 transmit (host memory -> card)
    • 2 receive (card -> host memory)
  - Xilinx FPGA Kintex-7: 7K410T – 5 total user FPGAs
  - 508,400 flip-flops per FPGA
    • 254K flips-flops with 6-input LUT
  - 1,540, 25x18 multipliers + 48-bit accumulator per FPGA
  - 1,590, 18 Kbit block RAM (2 Mbytes) per FPGA (or 445, 36 Kbit blocks)
    • Fully dual-ported
    • Each block RAM configurable as:
      • 32K × 1, 16K × 2, 8K × 4, 4K × 9 (or 8),
      • 2K × 18 (or 16), 1K × 36 (or 32), or 512 × 72 (or 64)
• 5 separate 256Mb x 16 DDR3 memories for each field FPGA
  - 3 memories PC3-1600
- 2 memories PC3-800
- Each memory has separate address, data, and control
- 6 separate 256Mb x 16 DDR3 memories for Dataflow Manager FPGA
  - 3 memories PC3-1600
  - 3 memories PC3-800
  - Each memory has separate address, data, and control
- Two independent low-skew global clock networks
  - distributed differentially and balanced
- Fast and Painless FPGA configuration via PCIe
  - On-board battery for AES bitstream encryption
- Full support for embedded logic analyzers via JTAG interface
  - ChipScope, Veridae, and other third-party debug solutions
- FPGA-controlled LEDs
  - Enough light to use as a LED-based flashlight
Description

Overview
The DNBFC_K7F5_PCIE is Xilinx Kintex-7 based FPGA board optimized for algorithmic acceleration applications requiring FPGAs with high performance local memory. Data movement to/from the FPGA grid is accomplished via a fixed 4-lane, GEN1/GEN2 PCIe bridge. Each field Kintex-7 FPGA (FPGAs labeled 1-4 in the block diagram) has five separate 256M x 16 DDR3 (4 Gb) memories. The Dataflow Manager FPGA (FPGA 0 in the block diagram) has six 256M x 16 DDR3 memories.

Dedicated PCIe, 4-lane controller (GEN1 or GEN2)
We ship the DNBFC_K7F5_PCIE with a fixed, full function, 4-lane master/target PCIe controller. The PCI controller has two mastering DMA engines, 2 for transmit (board -> host) and 2 for receive (host -> board). Drivers with 'C' source for several operating systems are included at no cost.

Kintex-7 FPGAs from Xilinx - Performance and Low Power
The Xilinx Kintex-7, 28 nm FPGAs are utilized. We use the second largest member of this cost effective (read: CHEAP) family. The Kintex-7 FPGA family has an impressive price/performance ratio for hardware-in-the-loop accelerators with excellent device power consumption properties. Operation frequency is approximately twice that of the previous low cost Xilinx FPGAs - Spartan-6.
Features of Kintex-7 include efficient, dual-register 6-input look-up table (LUT) logic, 36 Kb block RAMs, and second generation DSP slices which contain 25 x 18 multipliers along with a 48-bit accumulator.
We use the largest device from this family, the 7K410T in the FFG900 and FFG676 packages. 100% of the FPGA resources are dedicated to your application. All FPGAs, excluding the PCIe controller, are configured via PCIe. The PCIe FPGA can be updated in the field.

Memory – DDR3
The availability of large amounts of local high speed memory is pivotal to FPGA-based algorithmic acceleration applications. The DNBFC_K7F5_PCIE is optimized accordingly. Each of the four field FPGAs (FPGAs 1 thru 4) has a total of five, 4 Gb DDR3 memories. Each memory is 256M x16 with separate data, address and control. Three of these DDR3 memories are connected to FPGA pins capable of 800 MHz (1600 Mb/s per data pin) and remaining two are connected to FPGA pins capable of 400 MHz (800 Mb/s per data pin). The Xilinx Memory Interface Generator (MIG) works fine, so no separate memory controller IP is required. The five memories can be used independently or grouped in any manner that best fits your application. The Dataflow Manager FPGA (FPGA 0) has a total of six, 4 Gb DDR3 memories. Three of these memories are connected to FPGA pins capable of 800 MHz (1600 Mb/s per data pin) and three are connected to FPGA pins capable of 400 MHz (800 Mb/s per data pin).
As always, we provide examples and reference designs to help you with all of your memory interface issues. Please check with us to make sure that what we ship for no charge meets your requirements.

Power Consumption
The PCI Express specification limits slot power to 25 watts. The DNBFC_K7F5_PCIE is capable of consuming power significantly beyond that. In addition to the PCIe fingers, a separate connector adds a second path for power. This product is shipped with adequate heat sinks to consume TBD watts, but airflow is required in the chassis to dissipate the heat. Contact the factory if you require high reliability, no-fan heatsinks.

Status LEDs, Debug
Although no specific testing was performed, sophisticated statistical finite element models and back of the envelope calculations are showing the number of status LEDs to be bright enough to work as a flashlight. Contact the factory for more information about this sophisticated feature and make sure an adult is present during operation. These LEDs are user controllable from the FPGAs so can be used as visual feedback in addition to emergency lighting. A JTAG connector provides an interface to ChipScope and other third party debug tools.
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