DNK7_F5_PCIE
Hardware Manual
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2 Introduction

Congratulations on your purchase of a DNK7_F5_PCIE Algorithm Acceleration board!

This document attempts to address the typical questions and problems that a first-time user of a DNK7_F5_PCIE might encounter.

2.1 References

This document makes some reference to other pieces of documentation. These include:

- The board schematic. It is titled “Schematic_DNK7_F5_PCIE_503-0220-0000_Rev04.pdf” and should be found on your user CD.
- The board netlist. It is titled “dnk7_f5pcie_customer_netlist_rev04.net” and should be found on your user CD.

In many cases, these files capture more detail and are thus more useful than the H/W manual. These files will be referred to in many sections of this manual.

2.2 Terminology and Conventions

There is a variety of board-specific terminology that will be used through this document. Much of it will be defined in context, but there are some general terms/names that are useful to know.

- **gFPGA** – describes the four FF676-package Kintex-7 chips on this board. These are the “user FPGAs”, and are numbered F1 through F4. The block diagram in section 2 of this document displays the numbering convention for these FPGAs.

- **dFPGA** – this is the “dataflow manager” FPGA, the Kintex-7 FF900 package with a high-speed connection to the pFPGA (described below) and six DDR3 memories.

- **pFPGA** – this is the “PCI Express” controller on this board.

2.3 Warnings

To prevent damage to the boards, don't do the following:

- Don’t plug and unplug the board into live connectors, make sure your system/power supply is powered off before plugging and unplugging boards.
- Shake or physically shock the chassis while the board is installed. The mass of the heatsink may cause damage to the board if the chassis is forcefully moved. It is recommended to unplug and carefully transport the boards separately from the rest of the chassis.
3  **Quick Start Guide**  
This section of the guide details how to bring up and begin playing with your DNK7_F5_PCIE board. It is recommended that users unfamiliar with Dini Group products or FPGA boards in general follow the instructions, so as to familiarize oneself with the board and avoid common board bring-up mistakes.

1. **Setting up your Board**  
Skip this step if your board is already in a chassis.

Before unwrapping the board, please put on a static grounding strap, to prevent ESD damage to the board.

![Illustration of the top side of the board (without heatsink installed)](image)

Plug the board into your host system. Although the board uses a 4x electrical PCIe connection, a 16x slot is required for mechanical compatibility.

Plug in a 6-pin “PCI Express Graphics” power cable into the connector in the top-right corner of the above illustration.

3.1  **Power on and configuration**  
Power the system on. A green LED near the power connector should light when power is applied.

3.2  **Status LEDs**  
If possible, check the status LEDs that are visible through the PCI Express bracket. The LOS LED (red) should be off, and the LINK LED (green) should be on.
3.3 Loading the Driver & Running the Board

3.3.1 Linux Environments
From the USB flash drive, copy the aetest folder into your home folder. Enter linuxdrv-2.6 and type “make”. Then type “sudo sh dndev_load.sh”. The driver should load.

Note that you may need to install your kernel header files and gcc/g++ to compile the driver correctly. If you have trouble running the “make” command, contact support@dinigroup.com; include the output of the command in your email and we will help you resolve the compilation problem.

3.3.2 Windows Environments
A windows driver binary is provided under the AETEST/wdmdrv folder. To install the driver, tell windows to “search for the best driver in the following locations” and point it to the “wdmdrv/drv” folder. See the file “wdmdrv/README.TXT” for more details on building the driver and installing it.

3.4 Running the self-test
You may want to run our production built-in test on the board, to verify that the board has not been damaged during shipping and installation.

Under linux it is first necessary to build the AETest binary. Point your terminal to AETEST/aetest and type “make”. Under Windows you may use the pre-built “aetest_wdm.exe” executable.

For both operating systems, the rest of the test procedure is identical. Run the AETEST executable (aetest_linux or aetest_wdm.exe) with the command-line flag “-selftest”. The self test takes about 15 minutes to run and will print lots of output. However, a helpful summary is available at the end; it should report “all tests passed” or “some tests fail”. The log should be something like the below; the important parts to look for are highlighted.

---AETest Release 2---
Found Device --- v17df, d1909 name="DNK7F5 Kintex7 PCI Express 4 lane Board"

```
test_log: NOTE : Starting production test on DNK7F5_PCIE board : m_dnkJf5pcie.cpp 1323
test_log: NOTE : Vendor ID: 0x17df, Device ID: 0x1909 : m_dnkJf5pcie.cpp 1325
...

test_log: NOTE : Starting EMC test : m_dnkJf5pcie.cpp 1687
test_log: NOTE : Connected to PCIe bus: 4 lanes, Gen2 (0x10420040) : m_dnkJf5pcie.cpp 2574
test_log: NOTE : Writing EEPROM : m_dnkJf5pcie.cpp 3574
test_log: PASS : Passed all tests in this 4lane Gen2 PCIe slot : m_dnkJf5pcie.cpp 2582
```

```
test_log: NOTE : All tests passed : m_dnkJf5pcie.cpp 1632
Completed Self-test
press key
```

Please contact support@dinigroup.com if you have failing tests when running this procedure. Make sure to include the entire test log with your email.

### 3.5 Re-Programming the pFPGA over JTAG

If the pFPGA PROM gets corrupted, for example, due to an error during firmware upgrade over PCIe, it may be necessary to re-program the PROM over JTAG. The board must be powered during this process. Typically this is only necessary to recover from an unsuccessful firmware upgrade; firmware upgrades are usually performed using the AETEST software over PCI Express.

*Note: Xilinx iMPACT version 14.2 is known to have issues with programming the pFPGA BPI flash correctly. Please use Xilinx iMPACT 13.4 or 14.3 if possible.*
1. Connect a Xilinx JTAG cable to the JTAG header, circled below. Install Jumper J4 near the JTAG header.

Run Xilinx Impact. You should see the following screen, depicting the JTAG “chain” 7 devices. The LX75T is the device you will be programming.
2. Right-click on the part, and select “Assign configuration file”. Select the *.bit file you want to program into the board, and hit OK. On the user CD / flash drive, the firmware file can be found under FPGA_Reference_Designs\Programming_Files\dn0220_dnk7_f5pcie\pcie_config\LX75T\pcie_config.bit.

3. iMPACT will then open a prompt to add a BPI flash. Select “Yes”. Xilinx will bring up a file selection dialog. Select the *.mcs file you want to program into the board, which should be in the same directory as the .bit file.

4. Right-click on the newly added FLASH and select ‘Set programming properties’. Select “automatically load FPGA with currently assigned bitstream” for the “After programming Flash...” value.

5. Now, right-click on the FLASH part and select “Program”. Make sure to check “Verify”. The programming takes a few minutes but should complete successfully.

6. Power off the board and remove J4. The next time the board is powered on, the pFPGA should configure automatically from FLASH.
4 On-Board Interfaces

This section details the on-board interfaces found on the DNK7_F5_PCIE. These interfaces are used for moving data around on the board, as well as controlling your design.

4.1 Block diagram

This is a high-level block diagram of the board. It will be referred to in this section.

![Block diagram of the DNK7_F5_PCIE](image)

4.2 Chip-to-Chip Bus, “Horizontal”

The horizontal chip-to-chip bus connects adjacent pairs of FPGAs. It is the dark-blue bus in the above diagram, connecting chips F0 to F1, F1 to F2, etc. in a ring topology. The bus is 44 bits wide, allowing the user to implement a 32 bit interface and have a few pins left over as control signals.

The pinout is the same between all “horizontal” busses, with the exception of the pins selected on the dFPGA. This means that, for example, net “FPGACTC_F1F2_00” connects to pin U1.B9 and U2.N16, therefore, “FPGACTC_F2F3_00” will connect pins U2.B9 and U3.N16, and so forth. The purpose of this convention is to allow the user to have a single design with the same pin mappings loaded into FPGAs F1 – F4.
This bus is routed and timed to run at (at least) 200MbpsMHz “DDR”. This assumes source synchronous clocking in each direction. The clock signals are FPGACTC \_F<n>F<n+1>_CKp / FPGACTC \_F<n>F<n+1>_CKn in the “up” direction and FPGACTC \_F<n+1>F<n>_CKp / FPGACTC \_F<n+1>F<n>_CKn in the down direction. For example, FPGACTC \_F0F1_CKp/ FPGACTC \_F0F1_CKn are used to clock signals going from FPGA F0 to FPGA F1, and FPGACTC \_F1F0_CKp/ FPGACTC \_F1F0_CKn are used to clock signals going in the opposite direction.

For the clock signals, make sure to use the signal standard “DIFF_HSTL_I”. See the reference design for exact syntax on how to declare these pins. The rest of the bus may be run with signal standard “SSTL15”. Using the UCF provided with the reference design is probably the best way to ensure the correct signaling standards are used.

4.3 SF Bus

The SFB (Super-Fast Bus) is an 8-bit bus connecting the four gFPGAs to the pFPGA. The function of the pins is fixed based on the design loaded into the pFPGA. This bus is intended for communicating between PCI Express and the user FPGA in applications where a low-speed, low-latency interface is desirable. The bus pins are shared with the gFPGA SelectMAP configuration bus, thus, interleaving configuration and normal operation is difficult on the DNK7_F5_PCIe, and it is recommended that all FPGAs be configured before the SFB is used.

The SFB pins are constrained in the UCF; the net names start with “BUS_SFB”. LVCMOS18 signaling is used. The MBCLK network is used to clock SFB communication in a system-synchronous manner.

For a more detailed description of the timing, the exact pins used on each FPGA, and of the logical function of the SFB interface, please see the reference design, specifically the sfb_user_interface module, and/or the Software Manual for the DNK7_F5_PCIE.

4.4 DDR3 Discrete Chips

The DNK7_F5_PCIE gives all FPGAs (except the pFPGA) dedicated DDR3 SDRAM memory for user application. The Xilinx MIG IP core is intended to be used with these DDR3 SDRAM interfaces; the IP block may be generated via Xilinx coregen directly or the provided modules from our reference design may be used.

The physical pinout on the chips is designed to be completely compatible with the Xilinx MIG IP core requirements. The on-board routing should fully comply with the routing rules given in the Xilinx MIS documentation (UG586) to ensure that the DDR3 signals will have sufficient signal integrity to operate at 800MHz (1600mbps per pin effective).

The DNK7_F5_PCIE uses dynamic ODT for the DDR3 interfaces. See Xilinx AR 46082 for details about the use of dynamic ODT with 7-series devices.

Note that on some FPGAs, the CSn pin is pulled high by a pull-up resistor on the board. The user should make sure to actively drive the CSn signal in their design.
Most of the DDR3 functionality is reference design related, and hence a full description of the interface is outside of the scope of the H/W manual. Please see Xilinx UG586 “Memory Interface Solutions”, the DNK7_F5_PCIe Software Manual, and/or reference design for more details on this interface.

4.5 **MB Connections**
There are 6 connections shared between the four gFPGAs, these nets are called FPGACTC_MB[5:0]. They have no defined function and are for users to use.

4.6 **FPGA ID**
All four gFPGAs have a set of three pins beginning with “CHIPID”. These contain a binary encoding for the FPGA number (1-4) of the gFPGAs. They are intended for applications where the same bitfile is loaded into all four gFPGAs, but the bitfile must be able to determine which FPGA it is loaded into.

4.7 **Soft Reset**
The signals SOFT_RESETn is intended to provide a global “logic reset” for all five user FPGAs. It may be asserted from host software via the “-resetn=1” option and de-asserted via the “-resetn=0” option.
5 Clocking

There are three clock networks on the DNK7_F5_PCIE. This section describes their function.

1. DDR3 Clock Networks

There are two DDR3 clock networks – HPCLK and HRCLK. The nets on these networks begin with “CLK_HPCLK” and “CLK_HRCLK” respectively. These clock networks are intended to provide the reference clock (Xilinx calls this “SYSCLK” which has nothing to do with the DNK7_F5_PCIE SYSCLK clock network) for the MIG DDR3 DRAM controllers. HPCLK uses HSTL15 signaling and HRCLK uses LVDS signaling; both clocks start up at 200MHz although the frequency may be changed via AETEST.

This clock is distributed but NOT length-matched to all FPGAs, and should be received with the signaling standards mentioned above. Internal termination should not be used for these clocks; external on-board termination is provided.

5.1 SYSCLK Clock Network

The SYSCLK clock network is driven by gFPGA F1 (nets CLK_SYSCLK_HSTL_SOURCEp and CLK_SYSCLK_HSTL_SOURCEn) and should be received with the LVDS signaling standard. The intention of this clock is to be used as the general purpose logic clock. An MMCM or PLL may be used in the gFPGA to synthesize a wide range of frequencies; the exact implementation is left up to the user.

The distribution buffer on this network can output any frequency from DC up to beyond 1GHz, which is well above the limit of the FPGA’s global clock networks. This clock is distributed and length-matched to all FPGAs. External termination for this clock is provided at the FPGAs and therefore internal termination should be left disabled.

5.2 MBCLK Clock Network

The MBCLK clock network is driven by the pFPGA, at a frequency of 50MHz. This clock is “fixed frequency” and is derived from the PCI Express reference clock. Thus, if you are running the board without having PCI Express plugged in, this clock will not function. This clock is used as the system-synchronous clock for the SFB interface, among other functions, in the reference design.

This clock is distributed and length-matched to all FPGAs, and should be received with the LVCMOS18 signaling standard. No internal termination needs to be used.
6 Off-Board Interfaces

There is one primary off-board interface on the DNK7_F5_PCIE: the PCIe (finger) interface. The PCI Express interface is intended to move large amounts of data between the board and the host system. The JTAG interfaces allow direct communication to the FPGAs, for configuration or debug. This section will discuss these off-board interfaces.

The following picture shows the physical position of each of the interfaces.

![Board interfaces, color coded: PCIe fingers, JTAG](image)

6.1 PCI Express Interface

The PCI Express interface is the primary method of communication between the board and the host. The DNK7_F5_PCIE implements a fully compliant 4-lane GEN2 PCI Express interface (backward-compatible with GEN1), and provides board-specific drivers and software; driver installation and basic software use is described in section 3.3.

For more information on the PCI Express interface, please see the Software Manual for the DNK7_F5_PCIE.

6.2 JTAG ports

There is a single JTAG port on the DNK7_F5_PCIE, shared between the pFPGA, the system monitor CPLD, and the user FPGAs. Neither the pFPGA nor the CPLD should be programmed unless performing a "board recovery" procedure under Dini Group guidance; improper use of this interface may result in a non-functioning board. The gFPGA/dFPGA portion of the chain, however, may be used to configure FPGAs and perform debugging via utilities such as Xilinx ChipScope.
The JTAG ports may be interfaced to via a 14-pin Xilinx JTAG interface, using a cable such as Xilinx Platform Cable USB II. Links to distributors may be found at the Xilinx Virtex Board Accessories page. Tools such as iMPACT may be used to scan the chain - they should output something like the following:

![iMPACT Screenshot]

The first device in the chain will be the dFPGA, and the next four will be the gFPGAs. If you have fewer than 4 gFPGA installed on your board, the chain will be shorter (uninstalled FPGAs will not appear). Using iMPACT, you can manually program the gFPGAs one at a time (slow) or read back configuration information or debug status. Tools such as Xilinx Chipscope may aid the user in debugging his/her design inside the FPGA.

### 6.3 LEDs

There are two LEDs on each user FPGA, and three on the gFPGA. The LEDs are driven by FETs which have their gates attached to FPGA I/O pins – to cause an LED to light, drive the FPGA output high.

The dFPGA LEDs are placed on the PCIe card edge bracket and may be seen from outside the chassis. The user FPGA LEDs are scattered along the solder side of the board.
7  **Power and Cooling**

The DNK7_F5_PCIE features dense logic which requires extensive power management. The board is capable of exceeding the PCI Express 25W limit even with a moderate design loaded. Thus, attention to the power distribution and dissipation limitations of the DNK7_F5_PCIE is paramount to any user wishing to maintain a fast yet stable system.

7.1  **Power Connectors**

There is only one power connector on the DNK7_F5_PCIE, the PEG power connector in the north-east corner of the board. This connector should be connected to a power supply rail capable of supplying the entire power budget for the board; the power budget is highly user design dependent but can be up to 150W.

7.2  **Power Sequencing Requirements**

When running a power-intensive design, bringing the entire design out of reset puts an extreme load step on the power supplies. Thus, it is advisable, for a high power design, to bring the FPGAs out of reset in 50ms intervals or longer, rather than bringing them all out of reset at once, especially if you are having problems with the board resetting as the parts come out of reset.

7.3  **Power Distribution**

The DNK7_F5_PCIE has several high-power voltage rails used for internal FPGA logic and I/O power. The relevant ones to the user are:

+VCCINT - VCCINT power for FPGAs F0-F4, F7-F11. 30W max. per FPGA

+1.5V - VCCIO power for all FPGAs. 45W max.

If you are running an "aggressive" design or are experiencing voltage droop or spontaneous FPGA deconfiguration, try running your design through the XPE (Xilinx Power Estimator) spreadsheet. Make sure that your VCCINT and VCCIO requirements can be met by the on-board power supplies, as outlined above.

7.4  **Power Dissipation**

The flip-side of power distribution is power dissipation. All of the power that your design consumes is shed in the form of heat. Heat must be managed so as to stay within the operating temperature range on the Kintex-7 devices on the DNK7_F5_PCIE.

There are four primary variables to be concerned with that will affect the heat dissipation capability of the board. These are

1. Part grade, industrial vs commercial
2. Heatsink type and size (active vs. passive and height)
3. Chassis and fan type, for determining effective LFM of the board
4. Ambient Air temperature of the chassis

The DNK7_F5_PCIe passive heatsink requires at least 300LFM of airflow at no more than 40C (at the leading edge of the board) to be blow across the long axis of the board. Most server chassi designed for Nvidia Tesla™ boards should provide this amount of airflow. In systems not designed for high-power passively cooled boards, it may be necessary to add a fan to blow ambient air across the board.

7.4.1 On-board Temperature Sensors

There are several on-board temperature monitors on the DNK7-F5_PCIe, capable of reporting both the PCB temperature and the die temperature of the FPGAs. These can be queried using the “-info” argument for the AETEST command-line host software.

When a user design is loaded, it is also possible to read back the die temperature from the XADC hardware in the Kintex-7 FPGAs. This is preferable as the internal temperature readback is less susceptible to interference from I/O and internal logic activity. Please see the reference design for an example of how to implement the XADC primitive and connect it so that the internal FPGA temperature can be read from the user FPGA XADC by the AETEST software.

The board will reset the FPGAs when they reach 100C. This is below the absolute maximum rated temperature (where the parts will be damaged) but above the recommended maximum for commercial parts; at temperatures higher than 85C, commercial parts cannot guarantee timing of their logic. It is recommended that the die temperature for the FPGAs on the DNK7_F5_PCIe be maintained below 85C.

7.5 Battery Back-up

There is a battery for storing a battery-backed encryption key in the FPGAs. This is useful if you intend to use encryption-protected bitfiles. The battery, type SR44, is to be installed in the socket provided, near the PEG header.

7.5.1 Checking & Replacing the Battery

*Location of Battery Socket*
It is recommended that the battery be checked and replaced if necessary every year with the board in service. High temperatures may adversely affect battery life, if the board is housed in a chassis it may be advisable to probe the battery voltage more often. To check the battery voltage, probe the metal battery case (+) using ground as a reference. The batteries start at +1.5V nominal; a voltage below +1.2V suggests the battery should be replaced.

If you don't need to keep the encryption keys, then the battery may be replaced by remove the old battery and installing a new one, with the board powered off. If the keys in the FPGA must be kept, battery replacement should be performed as follows. Before removing the old battery, wire in a +1.5V voltage source to TP28 (a battery is fine too). Remove the old LR44 battery, and install a new one. The battery at TP28 will continue to power the +VBATT rail while the battery in the socket is replaced. There is no danger of significantly changing the LR44 battery as there is an in-line 10KΩ resistor in series with the battery to protect against this.

7.6 Cleaning Heat-Sinks
The heat sinks should be cleaned to maintain optimal heat transfer characteristics. Depending on how dusty the environment, cleaning may be necessary anywhere from once every few years to every few months.

To clean the heat sinks, power off your system, open up the board chassis, and examine the heat sinks. If there is significant dust build-up in the heat sinks, use compressed air to remove the dust. Compressed air can be bought at any electronics store, and is often advertised for just this purpose of removing dust.