Features

- Single Altera Stratix II GX FPGA (1152FBGA):
  - EP2SGX90E-5, -4, -3
  - 100% FPGA resources available for user application
  - Nearly 600k ASIC gates (LSI measure for 2SGX90)
  - Daughter card to DN8000 & DN7000-series products
- 7 separate FPGA clocks
  - 8-pin, socketed user clock
  - 125MHz
  - 2 factory-selectable LVDS oscillators
    - 53.12MHz to 700MHz
    - 200MHz (intended for DDR2)
    - 78.125MHz or 156.25MHz (selectable)
    - for SATA
  - SMA input (50 ohm)
- 12 High Speed Transceiver Channels
  - 622Mbps to 6.375Gbps
  - 4 SFP Sockets
  - 4 SMA Channels (Differential Rx/Tx)
  - 2 SATA (1 Host and 1 Peripheral)
- DDR2 SODIMM (200MHz)
  - 64-bit data width, 200MHz operation
  - PC2-3200/PC2-4200
  - Addressing and power to support 2GB
  - Verilog/VHDL reference design provided (no charge)
  - DDR2 SODIMM data transfer rate: 25.6Gb/s
  - Alternate SODIMM’s available:
    - QDR SSRAM
    - SSRAM pipeline/flowthrough, NoBL/ZBT
    - FLASH
  - Mictor connectors
  - Micron RLDRAM
- 4-megabit Serial Flash
  - Atmel AT45DB041B
- 8 Status LED’s - enough illumination to freeze a gazelle
- RS232 Connector and voltage translator
- Standalone operation with off-the-shelf ATX power supply
- Dual, 400-pin expansion connectors with 186 signals
  - Top and bottom of PWB (shared signals)
  - LVDS or single-ended signaling
  - Power, clocks, reset
- Full support for embedded logic analyzers via JTAG ByteBlaster II interface
  - SignalTap II and other third party tools

Block Diagram
Description

The DNMEG_S2GX is a daughter card that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DNMEG_S2GX is hosted on any DN8000 or DN7000-series ASIC Emulation product from The DINI Group, but can be used stand-alone. The DNMEG_S2GX is factory stuffed with the Altera's StratixII GX 2SGX90 (speed grades -5, -4, or -3) and can emulate >600k gates of logic as measured by LSI. This number does not include the embedded memories and DSP blocks resident in the FPGA. A high I/O-count, 1152-pin, flip-chip BGA package is employed, providing for abundant interconnects to the host and assorted peripherals. One DDR2 SDRAM SODIMM is provided, allowing the StratixII GX FPGA to address up to 2GB of memory. Alternative SODIMM's are available, including QDR SSRAM, SSRAM pipeline/flowthrough, NoBL/ZBT, FLASH, Mictor connectors, and Micron RLDRAM. The DDR2 SODIMM socket is tested at 200MHz, and reference designs are provided. A total of 186+ test pins (plus clocks and power) are provided on the top and bottom of the PWB via two high performance 400-pin expansion connectors. Reference material such as DDR2 SDRAM controllers and PCI drivers (with source) is included (in Verilog, VHDL, C) at no additional cost.

All 12 high-speed transceiver channels are utilized. Four channels are connected to SPF sockets, enabling a vast list of third party physical layer interfaces. Four channels are connected to SMA's. The remaining two channels are connected to a SATA Host and SATA Peripheral connector. All channels are tested and characterized to 6.375Gbps.

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Available Speed Grades (slowest to fastest)</th>
<th>ALM’s</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Max I/O’s</th>
<th>FF’s in I/O pad</th>
<th>Multipliers (18x18)</th>
<th>Memory (per FPGA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2SGX90E</td>
<td>-5,-4,-3</td>
<td>36,384</td>
<td>72,768</td>
<td>1,020</td>
<td>610</td>
<td>558</td>
<td>7</td>
<td>4,520,448</td>
</tr>
</tbody>
</table>

* -- 14 gates per LE/FF

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