Features

- QSFP+ socket
  - 4 ports 10GbE LAN/WAN using SFP+ modules OR
  - 1 port 40 GbE
- Hosted in an 4-lane GEN1/GEN2/GEN3 PCIe slot
  - 16-lane mechanical
  - Low profile, short length form factor
  - GEN1/GEN2 PCIe bridge provided
  - GEN3 supplied by user
- Fully compatible with our TCP Offload Engine (TOE)
- FIX board support package (DN_FBSP). Functioning reference design with:
  - 10 GbE MAC and 40 GbE MAC
  - TCP/IP Offload Engine (TOE)
  - FIX protocol parser
  - PCIe Interface (4-lane, GEN2)
  - Memory
    - QDR2 II+ Controller
    - DDR3 Controller
- Xilinx Kintex-7 FPGA (FFG676):
  - 7K410T-3,-2,-2L (fastest to slowest)
  - 7K325T-3,-2,-2L
  - 3M ASIC gates (ASIC measure) when stuffed with Kintex-7 7K410T
    - 254k flip-flop/6-input LUTs (708k total FFs)
    - 3.578 Kbytes total FPGA block memory (1590, 18 kbit blocks)
    - 1540, 25x18 multipliers

- Bulk memory: DDR3 VLP Mini-uDIMM
  - 72-bit data width (64-bit with 8-bit ECC)
  - 666.5 MHz operation, PC3-10600 (single rank)
  - Addressing/power to support 4GB
- DDR3 interface compatible with Vivado MIG
  - Optimized DDR3 controller for lowest latency bulk memory access
  - Optional RLDRAM Mini-uDIMM instead of DDR3 for ultra low latency
- QDR II+ SRAM memory: 4M x 18 (72Mb)
  - Separate 18-bit read and write ports
  - 500 MHz bus operation, DDR (double data rate)
    - Fast enough to be clocked at 312.50 MHz
    - Eliminates clock synchronization delays between memory and Ethernet clock
- SMBus-based thermal management
- GPS input for precise message time stamping and tracking
- Full support for embedded logic analyzers via JTAG interface
  - ChipScope and other third-party debug solutions:
    - Tektronix Certus
- Eight FPGA-controlled LEDs
  - Enough light to make your houseplants happy.

Table 1: FPGA Resources

<table>
<thead>
<tr>
<th>Kintex-7 FPGA</th>
<th>Speed Grades (slowest to fastest)</th>
<th>LUT Size</th>
<th>FF's</th>
<th>Gate Estimate</th>
<th>Max I/O's</th>
<th>Multipliers (25x18)</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Max (100% util) (1000's)</td>
<td>Practical (60% util) (1000's)</td>
<td></td>
<td>Blocks (18kbits)</td>
</tr>
<tr>
<td>7K410T</td>
<td>-2,-3</td>
<td>6-input</td>
<td>508,400</td>
<td>4,881</td>
<td>2,930</td>
<td>500</td>
<td>1,540</td>
</tr>
<tr>
<td>7K325T</td>
<td>-2,-3</td>
<td>6-input</td>
<td>407,600</td>
<td>3,913</td>
<td>2,350</td>
<td>500</td>
<td>840</td>
</tr>
</tbody>
</table>
Block Diagram

Description

Overview

The **DNPCIe_10G_K7_LL_QSFP** is a PCIe-based FPGA board designed to minimize input to output processing latency on 10-Gbit or 40-Gbit Ethernet packets. The primary application is for low-cost, low latency, high throughput trading **without** CPU intervention. Every possible variable that affects input to output latency has been analyzed and minimized. Raw 10 or 40 GbE Ethernet packets can be analyzed and acted upon without a MAC, interrupts, or an operating system adding delay to the process. This configurable hardware computing platform has the ability to achieve the theoretical **minimum** Ethernet packet processing latency.
The FPGA – The Xilinx Kintex-7

We use a single FPGA from the Xilinx Kintex-7 in the FFG676 package. This package supports 400 I/O with the majority utilized. Most are dedicated to off chip memory peripherals including a single QDR II+ for low-latency high speed look-up, and DDR3 Mini-uDIMM for performance oriented bulk storage. The Kintex-7 FPGA contains high-speed transceivers capable of 10GbE without need for an external PHY. Four of these transceivers are used for 4-lanes of GEN2/GEN3-capable PCIe. Four of the transceivers are connected to a single QSFP+ socket.

Two possible FPGAs can be stuffed: 7K410T or the 7K325T. Both FPGAs come in a variety of speed grades (-2/2L, -3) with -3 the fastest. The -1 speed grade is not rated for 10 GbE transceiver operation, so isn’t applicable to this application. Table 1 depicts the resources of the two FPGAs with the Xilinx marketing exaggerations ruthlessly amputated. These are both large, but low-cost FPGAs. The 7K410T is capable of handling ~3M ASIC gates of logic, with the 7K325T capable of ~2.3 million gates. Features of the Kintex-7 FPGAs include efficient, dual-register 6-input look-up table (LUT) logic, 18 Kb (2 x 9 Kb) block RAMs, and second generation DSP48E1 slices (includes 25 x 18 multipliers). Floating point functions can be implemented using these DSP slices.

Four Channels of 10 GbE or a single channel of 40 GbE

The Kintex-7 FPGA has transceivers capable of 10 GbE. The physical interface is handled using a single QSFP+ module. This allows you to bypass a MAC if necessary and process raw Ethernet packets.

QDR II+ SSRAM – Memory with the lowest latency

We use a single quad data rate static RAMs (QDR II+ SSRAM) in the 4M x 18 size (72Mbit). This type of memory has separate input and output data paths enabling maximum read/write data bandwidth with minimum latency. The maximum tested frequency of this memory is 400 MHz. To minimize processing latency, we suspect it will be best to clock this QDRII+ SRAM at 312.50 MHz, exactly twice the internal Ethernet controller frequency of 156.25 MHz. The Kintex-7 FPGAs are capable of generating internal 2x clocks that are phase synchronous, eliminating the latencies associated with the tricky re-synchronization of data moving between different clock frequencies. The internal controller can be optimized in any way you choose. We, of course, provide several verilog examples for no charge that you are welcome to use. All functions of the QDR II+ SSRAM can be exploited, including concurrent read and write operations and four-tick bursts. The only real limitation is the amount of time and effort spent in customizing the individual memory controllers.

DDR3 – A large amount of local, bulk memory

A single PC3-10600 DDR3 VLP Mini-uDIMM socket enables up to 4GB of memory for bulk storage and lookup. Assuming a 4GB DIMM, the memory configuration is 512M x 72. Using a -2 or -3 speed grade FPGA, this interface is tested at the maximum FPGA I/O frequency: 666.5 MHz (1333 Mb/s with DDR). You are welcome to use this memory as 64-bits with 8 bits of error correction (ECC), or as a 72-bit memory without correction.

To minimize data synchronization across clock boundaries, it probably makes sense to clock this DDR3 interface at a 3x multiple of the base Ethernet frequency of 156.25 MHz, which is 468.75 MHz. A 3x phase synchronous clock can be easily generated internal to the FPGA, allowing zero latency synchronous data transfers between the Ethernet packet receiving logic and the DDR3 memory controller. The DDR3 controller can be optimized in any way you choose. We, of course, provide several verilog examples for no charge that you are welcome to use. All functions of the DDR3 DRAM can be exploited and optimized. Up to 8 banks can be open at once. Timing variables such as CAS latency and precharge can be tailored to the minimum given your operating frequency and the timing specification of the exact DDR3 memory utilized. As with the QDRII+ SRAM, the only real limitation is the amount of time and effort spent customizing the DDR3 memory controller to your needs.

PCIe – Customizable 4-lane, GEN2/GEN3 PCI Express

PCIe is connected directly to the FPGA via 4-lanes of GTX transceivers. Note that the board has a 16-bit mechanical finger for stability. The interface is fully GEN2 and GEN3 capable. We ship GEN2 PCIe IP that is a full function, fixed, 4-lane master/target. If you want GEN3, you will have to supply the IP. To gain access to the PCIe interface, this IP must be integrated with your application. The Dini Group PCIe IP provides a flexible interface that allows the user access to multiple DMA engines, scratchpad memories, interrupts, and other endpoint-related functions to maximize performance while utilizing minimal FPGA resources. Drivers for ‘C’ source for several operating systems are included no charge.
How Everything Works ….

With direct data feeds such as NASDAQ ITCH and OUCH, the DNPCIe_10G_K7_LL_QSFP contains all of the basic functions required to minimize the amount of time it takes to receive Ethernet packets, process them, and respond deterministically. By using the FPGA to process Ethernet packets, the processor and operating system are removed from the critical path and traditional sources of latency such as interrupts and context switching no longer hinder performance. Not a single clock cycle. For algorithms requiring processing, FPGA resources can be hard coded to perform the task. This includes real-time Monte Carlo analysis, and floating point.

Photos

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