Features
- Quad QSFP28 sockets. Each socket:
  - 1 port 100 GbE or
  - 1 port 40 GbE or
  - 4 ports 10 GbE
- Dual Samtec FireFly™ for two additional interfaces
  - 100/40/10 GbE or board to board interconnect
- Hosted in an 16-lane GEN2/GEN3 PCIe slot
- Fully compatible with our optional TCP Offload Engine (TOE/TOE128/TOE_IoT)
- FIX board support package (DN_FBSP). Functioning reference design with:
  - 100GbE/40 GbE MAC/10 GbE MAC
  - TCP/IP Offload Engine (TOE/TOE128)
    - Up to 128 sessions
  - FIX protocol parser
  - PCIe Interface (16-lane, GEN3)
  - Memory
    - DDR4 Controller
- Intel Stratix 10 MX FPGA (F2597 FBGA)
  - MX2100 or MX1650
  - 16 million ASIC gates (ASIC measure) when stuffed with MX2100
    - 1.4M flip-flop/6-input LUTs (2.8 million total FFs)
    - FPGA memory (12,984, 20kbit blocks)
      - eSRAM: 90 Mbits
      - M20K: 134 Mbits
      - HBM2: 8/16GB
    - 7,920 multipliers – each 18x19
    - OpenCL (consult factory for availability)
- 2 external banks DDR4 Memory (260-pin DIMM)
  - up to 128GB each (2GB x 72)
  - PC4-2400
- Other custom DIMM options (consult factory for availability):
  - QDRII+, DDR3, RLDRAM
  - Mobile LPDDR SDRAM
- Full support for embedded logic analyzers via JTAG interface
  - Exostiv
- Eight FPGA-controlled LEDs
  - Enough debug LEDs for Emergency Vehicle & Strobe LED Lights

Description

Overview

The DNPCIe_400G_F1SM is a PCIe-based FPGA board designed to minimize input to output processing latency on 10-Gbit, 40-Gbit, or 100-Gbit Ethernet packets. The primary application of this board is the acceleration of data center tasks and algorithms. This list includes low-cost, low latency, high throughput trading without CPU intervention and search engine acceleration. Every possible variable that affects input to output latency has been analyzed and minimized. Raw 10/40/100GbE Ethernet packets can be analyzed and acted upon without a MAC, interrupts, or an operating system adding delay to the process. This configurable hardware computing platform has the ability to achieve the theoretical minimum Ethernet packet processing latency.
Block Diagram

DNPCIe_400G_F1SM Intel Stratix 10 MX FPGA PCIe (GEN3) card with quad QSFP28 (100/40/10GbE)

DNPCIe_400G_F1SM
Monster's Evil Bowl of Clam Chowder
Block Diagram
v1.00
The FPGA – Intel Stratix 10 MX

We use a single FPGA from the Intel Stratix 10 MX family in the F2597 package. This package supports 656 I/Os with the majority utilized. Most are dedicated to off-chip memory peripherals including 2 separate banks of DDR4 memory. Sixteen of transceivers are used for a 16-lane GEN3 PCIe interface. Sixteen of the transceivers are connected to four QSFP28 sockets each can be configured as 40/100GbE Ethernet or 4 channels of 10 GbE.

You can choose one of two Stratix 10 MX FPGAs: MX2100 or MX1650. These FPGAs come in a variety of speed grades -1, -2, -3 with -1 the fastest. Table 1 depicts the resources of the FPGA with the Altera marketing exaggerations removed. The MX2100 is capable of handling nearly ~16M ASIC gates of logic using a reasonable measure. These are large FPGAs. Power and cooling could be the constraining variable for resource utilization and clock frequency. This gate count number does not include the internal FPGA memory and multiplier blocks that are free, whether you use them or not. Features of the Stratix 10 MX FPGAs include efficient, dual-register 6-input look-up table (LUT) logic, several different variations of internal block RAMs, along with abundant 18x19 multipliers. Direct support for many floating operations is a key advantage of the Stratix 10 MX FPGA fabric. OpenCL will come just as soon as we figure out how to get this board into the program.

Table 1 -- FPGA Resources

<table>
<thead>
<tr>
<th>Stratix10 MX</th>
<th>Speed Grades (slowest to fastest)</th>
<th>LUT Size</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Multiplier s (18x19)</th>
<th>Tile</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Max (100% util) 1000’s</td>
<td>Practical (60% util) 1000’s</td>
<td></td>
<td>HBM DRAM (GB)</td>
</tr>
<tr>
<td>MX2100</td>
<td>-3,-2,-1</td>
<td>6-input</td>
<td>2,810,880</td>
<td>26,984</td>
<td>16,190</td>
<td>7920</td>
<td>2,3,5,4</td>
</tr>
<tr>
<td>MX1650</td>
<td>-3,-2,-1</td>
<td>6-input</td>
<td>2,276,800</td>
<td>21,857</td>
<td>13,110</td>
<td>6652</td>
<td>3,5,4</td>
</tr>
</tbody>
</table>

Low Latency Network Interface
Quad QSFP28 for 100/40/10 GbE

Four transceiver lanes are connected to each QSFP28 socket, enabling a single 100 or 40 GbE interface or four, 10 GbE interfaces. Raw Ethernet packets (UDP) can be accessed directly by bypassing the MAC. Dual Samtec FireFly™ connectors allow for two additional 100/40/10 GbE interfaces or can be used for board to board data communications.

Memory
DDR4 – 2 banks: Up to 128GB each

Dual 240-pin SODIMMs are mounted on the card, each providing up to 2GB x 72 of DDR4 memory (128GB). We can provide alternate memory in this socket including RLDARAM, SSRAM, QDRII+, LPDDR, et al. Contact the factory for the various options and lead-times.
PCIe – Customizable 16-lane, GEN3 PCI Express

PCIe is connected directly to the FPGA via 16-lanes of transceivers. The interface is fully GEN2 and GEN3 capable. We ship GEN3 PCIe IP that is a full function, fixed, 16-lane master/target. To gain access to the PCIe interface, this IP must be integrated with your application. The Dini Group PCIe IP provides a flexible interface that allows the user access to multiple DMA engines, scratchpad memories, interrupts, and other endpoint-related functions to maximize performance while utilizing minimal FPGA resources. Drivers (required) for ‘C’ source for several operating systems are included at no charge.