Product Brief
June 2013
Ver. 1.22

Features
• Cabled GEN1 PCIe-hosted logic prototyping system
  - 2 – Altera Stratix V FPGAs
  - 5SGXAB,A9,A7,A5 (largest to smallest)
  - for logic prototyping
  - 5SGSD8,D6
  - for signal processing
  - 100% FPGA resources available for user application
• 16.6M+ ASIC gates (reasonable ASIC measure) with two 5SGXAB
  - 7,852 – 18x18 multipliers with dual DDR3
• 4 configurable high speed serial interface card slots (IOB), 2 per FPGA
  - 12 – 14.1 GHz serial links per slot
  - 32 – general purpose I/O for out of band signaling (OOB)
• Options interfaces include:
  - 100 GbE Ethernet (via CFP module)
  - 40 GbE Ethernet
  - Quad QSFP+
  - Octal SFP+
  - GEN1/GEN2 PCIe
  - USB3
  - SMAs
• FPGA to FPGA interconnect is single-ended or LVDS
  - 700 MHz LVDS chip-to-chip DDR with -2 speed grade (1.4 Gb/s)
• Reference designs for integrated I/O pad shift registers
  - 10x FPGA to FPGA pin multiplexing per LVDS pair
  - Greatly simplified logic partitioning
  - Source synchronous clocking for LVDS
• 2 separate DDR3 SODIMMs, PC3-8500
  - 64-bit data
  - Addressing/power to support 4GB
  - DDR3 Verilog reference design provided (no charge)
  - VHDL on special request

- Optional RLDRAM DIMM instead of DDR3 for ultra low latency
- Marvell MV78200 Discovery Innovation Dual CPU
  - 1 GHz clock
  - Dual USB2.0 ports (Type B connector)
  - Dual Serial-ATA II connectors for 2 external hard drives (SATA II)
  - Gigabit Ethernet interface
  - 10/100/1000 GbE (RJ45)
  - Sheeva™ CPU Core (ARM v5TE compliant)
  - Out-of-order execution
  - Single and double-precision IEEE compliant floating point
  - 16-bit Thumb instruction set increases code density
  - DSP instructions boosts performance for signal processing applications
  - MMU to support virtual memory features
  - Dual Cache: 32 KB for data and instruction, parity protected
  - L2 cache: 512 KB unified L2 cache per CPU (total of 1MB), ECC protected.
  - 1 GB external DDR2 SDRAM
  - Organized in a 128M x 64 configuration
  - 400 MHz (800 MHz data rate with DDR)
  - RS232 port for terminal-style observation
  - After configuration, both CPUs dedicated entirely to user application
  - Linux operating system
    - Source and examples provided via GPL license (no charge)
    - ~15 seconds to CPU boot
  - 3 board-level global clock networks (GCLK[2:0])
    - Separate programmable synthesizers for each network (S15326)
    - Ultra-low jitter
  - 2, 400-pin MEG-Array connectors for daughter card expansion
    - 180 signals
    - 700MHz on all signals with source synchronous LVDS
    - Reset, presence detect
    - Supplied power rails (fused):
      - +12V (24W max)
      - +5V (10W max)
      - +3.3V (10W max)
  - Pin multiplexing to/from daughter cards with LVDS (up to 10x)
  - Auspy AES models for partitioning assistance
    - Hooks and models for other third-party partitioning solutions
  - Fast and Painless FPGA configuration
    - USB, PCIe, Ethernet et al.
    - Integrated sanity checks on configuration files
  - Custom base plate (standard) and optional rackmount chassis
    - Provides protection from those drooling engineers
  - Full support for embedded logic analyzers via JTAG interface
    - SignalTap, Veridae, and other third party debug tools
  - Convert MEG-Array expansion connectors to interconnect with the DNMEG_Intercon.
  - Enough status LEDs to function as a bathroom nightlight.

Description Overview
The DNS5GX_F2 is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DNS5GX_F2 can be operated stand-alone or can be hosted via USB, cabled PCIe, or Ethernet. A single DNS5GX_F2 configured with 2 Altera Stratix V 5SGXABs can emulate up to 16.5 million gates of logic as measured by a reasonable ASIC gate counting method. This ASIC gate estimate does not include the embedded memories and multipliers resident in each FPGA.
Overview (continued)
The DNS5GX_F2 achieves high gate density and allows for fast target clock frequencies by utilizing FPGAs from Altera's Stratix-5 FPGA family for logic and memory. All FPGA resources are available for the target application. Any subset of FPGAs can be stuffed and each FPGA position can be stuffed with any available speed grade. Four modular slots can add a variety of high speed interfaces, including 100 GbE, 40 GbE, 10Gbe, GEN1/GEN2 PCIE, USB3.0, et al.

Stratix V FPGAs from Altera
High I/O-count, 1932-pin, flip-chip BGA packages are utilized. Abundant interconnects are provided between the FPGAs. The 5SGXAB has a total of 840 I/O’s along with 48, 14.1-Gbps transceivers. All pins are utilized. FPGA to FPGA busses are routed and tested as unidirectional source synchronous LVDS to run at 700MHz+ (1.4 Gb/s with DDR). The LVDs signals can be split on a pair by pair basis and used single-ended at a reduced speed of about 225MHz. Example designs utilizing the integrated I/O block shift registers with DDR (double data rate) for pin multiplexing are included. Two separate high speed 40-pin busses (NMB0 and NMB1) connected each field FPGA to the Config FPGA and are optimized for data transfer.

Block Diagram
The Marvell MV78200 Discovery™ Dual CPU

A MONSTER for data movement and manipulation

Easy FPGA configuration is a required feature of large, multi-FPGA boards. We use an onboard CPU to handle this function. We chose a Marvell MV78200 from the Discovery™ Innovation CPU family. Bluntly stated, this CPU is massive, massive overkill for the mundane task of FPGA configuration. The MV78200 comes in a variety high performance interfaces, and all can be utilized to your advantage.

Dual Sheeva™ CPUs, 1GHz with floating point

And after we are done configuring the FPGAs we dedicate both CPUs to your application. The CPUs in the MV78200 are Marvell Sheeva™ cores, which are ARM v5TE compliant. The CPUs are clocked at 1GHz and each processor has a single and double precision floating point unit. A fixed 1 GB, DDR2 memory is standard and is useful for large amounts of high speed data buffering. The memory is organized as 128M x 64 and clocked at the full frequency allowed: 400MHz (800 MHz effective with DDR). This DDR2 bank is shared between the two CPUs. Boot code is resident in an SPI Flash, and application code is downloaded via any port: PCIe, USB, and Ethernet. We ship Linux as the standard operating system. Options exist for VxWorks and other real-time operating systems. Contact the factory for more information.

PCI Express

The Marvell 78200 acts as a two-port high-speed PCI Express switch (2.5Gbs). It connects both user FPGAs at 4-lane PCI Express speeds to a host computer. The Marvell 78200 has multiple DMA engines to pump data to and from any port. The user interface on the FPGA is a simple-to-use, pipelined address/data bus running at 6.4Gb/s. Drivers for data movement to and from a host machine are provided. A simple example FPGA design and host computer application streaming data at PCI Express x4 bandwidth to all seven FPGAs are provided.

Two Serial-ATA Ports (SATA II)

The MV78200 has two Serial-ATA Generation 2 (SATA II) ports, each capable of running at 3.0 Gb/s. SATA is intended for high speed data transfer to/from serial-ATA hard drives. Two SATA connectors are provided, allowing for direct, high-speed interfacing to external hard drives. The MV78200 has specialized enhanced DMA (EDMA) engines for HDD data transfer with 512-byte buffer for each channel. Examples of all possible data movement options, with source, are included.

GbE – 802.3 Gigabit Ethernet

The MV78200 can be controlled over its built-in Ethernet port. The interface is a standard RJ45 connector. This port can be used to configure FPGAs, set board clocks and other resources, and access the Linux terminal. This terminal can also be used to send data to and from the user FPGA design at gigabit Ethernet speeds.

MEG-Array Daughter cards

The DNS5GX_F2 is easily adaptable to all applications via daughter cards. Two separate 400-pin FCI MEG-Array connectors allow for customization via expansion. Signals to/from these cards are routed differentially where appropriate and can run at the limit of the FPGA: 700MHz. Clocks, resets and abundant (fused) power are included in each connector. Signals are routed from the FPGAs on a bank basis, and the daughter card selects the I/O voltage of the connector by driving the VccI/O of the FPGA bank. The I/O voltage ranges are +1.5V to +3.3V. If these expansion cards are not utilized, The DNMEG Intercon card can be used to convert these two connectors to FPGA to FPGA interconnect.

DDR3 UDIMM – A Large amount of local, bulk memory

A DDR3 SODIMM socket is connected to each FPGA. Address and power is provided for up to 4GB DDR3 of memory. With a 4GB UDIMM memory stick, the configuration is 512M x 64. The socket is tested to the PC3-8500 specification. Alternate SODIMM memories are in production, including an RLDRAM and a QDRII+ option.
High Speed Serial Interfaces – The IOB

The DNS5GX_F2 has 4 modular positions for customized high speed serial interface cards. These cards are called IOBs for ‘I/O boards’. Each position has an interface to 12, 14.1 Gbps transceivers, along with 32 general purpose I/Os for out of band signaling. Contact the factory for details, but you will be able to select from any of the following applications:

- 100 GbE Ethernet (via CFP module)
- 40 GbE Ethernet
- Quad QSFP+
- Octal SFP+
- GEN1/GEN2 PCIe
- USB3
- SMAs

Easy Configuration via PCIe, USB, or Ethernet

Configuration of the FPGAs is under the control of the Marvell CPU. Configuration data can be provided over PCI Express, USB, Ethernet, or on-board non-volatile memory. It can be copied to the board using a USB memory stick (provided). Configuration occurs automatically after the CPU boots. Sanity checks are performed automatically on the configuration files, streamlining the configuration process in the case of human error. Multiple LEDs provide instant status and operational feedback.

Laboratory testing is showing that the amount of light provided by the LEDs is enough to illuminate a small designer bathroom. As always, reference material such as DDR2 SDRAM controllers, flash controllers, et al. is included (in Verilog, VHDL, C) at no additional cost.

19" Rackmount Chassis

The DNS5GX_F2 comes standard mounted to a base plate and enclosed in a 19", 4U-high, rackmount chassis. The chassis is shipped with a Zippy Technology Corporation power supply rated at 600 watts with an AC input voltage range of 100~240 VAC. The front panel has an LCD display with an ON/OFF switch for power, and momentary switches for HARD RESET and LOGIC RESET. The front panel connectors support the following functions:

- MCU RS232 - FPGA configuration and control
- USB - Hosting and/or FPGA configuration
- User RS232 (2,3,4) - User RS232 ports (requires UART in FPGA)

#### Stratix-5 FPGA

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<th>Stratix-5 FPGA</th>
<th>Speed Grades (slowest to fastest)</th>
<th>LUT Size</th>
<th>FF's</th>
<th>Gate Estimate</th>
<th>Max I/O's</th>
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