A host interface is required and this IP package includes an integrated 4-lane GEN1/GEN2 PCIe bridge. Simulation models and test fixtures are included. This IP is optimized for low latency: the host CPU is NOT involved in payload data transfer. Not all TCP functions are handled in the IP. High complexity/low importance network features such as setup/teardown, ARP, ping, DHCP, et. al. are passed to a Linux driver via the PCIe interface. ‘C’ source for this driver is included, allowing customization. The user is responsible for presentation layer 6 and application layer 7 and can be implemented in the FPGA or elsewhere. All of the functions associated with TCP/IP layers 2, 3, 4, 5 (datalink, network, transport, and session) are implemented.

The maximum transmission unit (MTU) is 1536 bytes. CRC validation and checksum validation and reordering of out-of-order packets are done directly in the FPGA, along with packet retransmission upon error/lost/out of order packet reception. The TX and RX replay buffers are configurable: 4KB →64KB. Protection Against Wrapped Sequences (PAWS) is handled in the FPGA.

### Features
- **FPGA TCP Offload Engine (TOE) IP** for networking applications
- Minimum latency and deterministic latency
- Supplied as encrypted .nci (Xilinx) or optional verilog source
- Integrated PCIe bridge (required) provided in encrypted .nci format
- Complete simulation models and test fixtures
- Host CPU NOT involved in payload data transfer
- 0% CPU load during middle of TCP session - TCP data packets handled by TOE not passed to CPU
- Full 10GBE line rate - No Ethernet pause frames generated
- CPU required only for High complexity/low importance network features: Setup/teardown of TCP session - ARP, ping, DHCP, SMPT, et. al. - Linux driver with ‘C’ source included
- Layers 2, 3, 4, 5 (datalink, network, transport, and session)
- Layers 6, 7 (presentation, application) is user’s responsibility in FPGA
- MTU of 1536 bytes
- CRC validation and checksum validation
- Ethernet CRC validation - IP and TCP checksum validation - Reordering of out-of-order packets
- Nagle algorithm - Fast retransmit
- Optimized for lowest receive (about 13 clk cycles) and transmit latency (about 13 clk cycles) at 156.25Mhz. (2 RX longer latency, 5 TX longer latency - roughly). With store/forward latency in each direction.
- User selectable amount of internal FPGA ram for replay/buffers (4KB to 256KB).
- Optimized internal DRAM (DRAM) for increased size retransmit buffers.
- Can achieve >90% of the 10GBE bandwidth (in both transmit and receive) with a single module. Multiple modules can achieve 100% of the 10GBE bandwidth.
- Multiple TOE128's can be connected to the same Ethernet if 128 sessions in a single module (each session is a connection to 1 other computer).
- TCP/IP Features: - retransmit - MSS/MTU - RTT/persist/replay timers - TX/routing (optional) - server and client mode supported on each concurrent TCP/IP session - RFC793/791 - up to 64KBs per session for retransmit buffering - congestion control - RTO
- FPGA resources required: SRLCES assume about the same as TOE1 (approx 3% of Vx-565).
- RAMB36s: 28 to 105 depending on TX buffer size (3.5% to 13% of Kintex 410, or 3% to 12% of V6-565).
- Netfix for TOE128 and PCIe interface, verilog source for all other pieces
- Entire TOE128 design runs at 156.25Mhz. Clock domain change FIFOs are available for the user interface side so you can run it at a slower/faster frequency.
- Coming soon to a Dini board near you!
- Other items coming soon (contact factory for details): Dini 10G MAC low latency 40GBE support

### Product Brief

**September 2014 Ver. 1.0**

- Takes less than 50% of the FPGA (410).
- Congestion avoidance
- Packet retransmission upon error/lost/out of order packet reception
- 128 TCP/IP session per instantiated TOE. Additional TOE128s and TOE1 can be cascaded to support multiple sessions
- Limited only by FPGA resources
- Client or server mode
- Configurable TX and RX replay buffer
- 4KB → 64KB
- Protection Against Wrapped Sequences (PAWS)
- Configurable port number
- IPv4 with future upgrade path to IPv6/IPv6
- TIDB consult factor
- TCP timestamps for congestion avoidance (optional)
- Configurable timeout
- Initially targeted to the Dini Group DNPCI: 10G HX7 HX7 with Virtex-6 HX7
- Cost reduced Kintex-7 version available
- Altera Stratix version also available
- Direct interface to the Xilinx 10 Gigabit Ethernet Media Accessors
- Controller (10GEMAC/Interconnect)
- 64-bit bus interface
- Synchronous FIFO clocked at 156.25Mhz
- Does 128 TCP/IP sessions in a single module (each session is a connection to 1 other computer).
- Dini Group

**TCP Offload Engine IP (TOE128)**

For Latency Critical, FPGA-based Embedded Networking Applications

### Model 1: Xilinx .nci file

- Encryption of the interface
- Complete verilog source

### Model 2: Verilog Source

Verilog is our native language. This second distribution option gets you the complete source. You are not allowed to redistribute the source. The license agreement has all the details in the license agreement supersedes what is written here.

Under extreme duress and only under extreme duress, we will convert to VHDL. Should we do this conversion, please note that new features and bug fixes will be first available in Verilog. We really don’t like VHDL and all repeatable synthetics tools accept mixed language RTL anyway.

A maintenance contract, for bug fixes and feature enhancements is probably a good idea. 1 year is required at the time of purchase, with optional extensions sold on a yearly basis. Contact Dini sales for more details.

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**FPGA Resources Required**

<table>
<thead>
<tr>
<th>Module</th>
<th>FFS</th>
<th>LUTs</th>
<th>BRAMs</th>
<th>MBCG</th>
<th>GXT</th>
<th>%FFS(325T/410T)</th>
<th>%LUTs(325T/410T)</th>
<th>%BRAMs(325T/410T)</th>
<th>%SLICES(325T/410T)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOE128</td>
<td>128</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1.67% / 1.34%</td>
<td>4.40% / 3.52%</td>
<td>12.36% / 6.92%</td>
<td>12.36% / 6.92%</td>
</tr>
<tr>
<td>TX BUFFER(4KB)</td>
<td>181</td>
<td>14</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>0.04% / 0.04%</td>
<td>0.00% / 0.00%</td>
<td>0.67% / 0.38%</td>
<td>0.67% / 0.38%</td>
</tr>
<tr>
<td>TX BUFFER(256KB)</td>
<td>94</td>
<td>112</td>
<td>12</td>
<td>3</td>
<td>0</td>
<td>0.07% / 0.06%</td>
<td>0.67% / 0.38%</td>
<td>18.43% / 10.31%</td>
<td>18.43% / 10.31%</td>
</tr>
</tbody>
</table>

### TOE128 IP Distribution Model

The TOE128 is distributed in two different ways:

- • encrypted .nci file
- • complete verilog source

**Model 1:** Xilinx .nci file

An .nci file enables integration at the place and route stage into the Xilinx FPGA tools. Source is not provided, but full simulation libraries are supplied. You get this version when you get the FIX support package for our FPGA boards: DN FBSP. Required operating system driver functions and APIs are supplied, with source, in ‘C’ for Linux.

The TOE IP, supplied as part of the DN FBSP, is restricted to Dini products and will not operate on other FPGA-based boards. You are welcome to use this IP free of royalties or restrictions on Dini Group products. A single DN FBSP license is required for your company and allows your company to use it worldwide in any number of Dini boards and any number of applications.

**Model 2:** Verilog Source

Verilog is our native language. This second distribution option gets you the complete source. You are not allowed to redistribute the source. The license agreement has all the details in the license agreement supersedes what is written here.

Under extreme duress and only under extreme duress, we will convert to VHDL. Should we do this conversion, please note that new features and bug fixes will be first available in Verilog. We really don’t like VHDL and all repeatable synthetics tools accept mixed language RTL anyway.
Overview
TCP Offload 128 (TOE128) is a FPGA-based IP that receives and transmits Ethernet/IP/TCP packets on Ethernet networks across 128 simultaneous sessions. TOE128 delivers payload data, in order, to the user’s application with:

- Extra TCP/IP packet fields removed
- No missing data
- Verified by appropriate CRCs and checksums
- Flow control

The purpose is to offload the TCP/IP function from the CPU and perform it directly in FPGA-based hardware. TOE dramatically reduces the input to output response time and jitter by eliminating the need for host processor intervention when analyzing data packets. This IP is designed to be utilized in FPGA-based high frequency, low latency Wall Street trading applications. At the intended target frequency of 156.25 MHz, the TOE128 operates at the full 10Gbe line rate, generating no Ethernet pause frames.

What basic functions are required?

10 Gbe Media Access Controller from Xilinx
In minimum latency approaches, it is necessary to avoid using external PHYs since they add significant latency. This IP assumes an FPGA PHY is used. The Xilinx PHY needs a MAC, and the 10 Gigabit Ethernet Media Access Controller (10GEMAC) is required to use this TOE128 IP. You purchase this separately from Xilinx as it is not included. Note that Xilinx has a free version that disables itself after a few hours. This free version contains all of the functionality of the full version and can be used for evaluation.

The TOE128 IP can connect to the slower 1 Gbe MAC and we can make modifications here in La Jolla to interface the TOE128 to different MACs. Contact DINI sales for more information.

This Xilinx core is compatible with the Virtex-6 HXT FPGAs and works fine on both Virtex-7 and Kintex-7. Features of the Xilinx 10GEMAC include:

- Designed to IEEE 802.3-2005 specification
- Configured and monitored through an independent microprocessor-neutral interface
- Optional Statistics counters
- Configurable flow control through MAC Control pause frames; symmetrically or asymmetrically enabled
- Generate customized core using the CORE Generator™ technology
- Cut-through operation with minimum buffering for maximum flexibility in 64-bit client bus interfacing
- Ability to generate core with no physical interface to allow users to connect the PHY-side interface of the core to user logic
- Powerful EtherStats-based statistics gathering
- Programmable Interframe Gap
- Custom preamble preservation mode
- Supports Deficit Idle Control (DIC) for max. data throughput
- Maintains minimum IFG under all conditions and line rate performance
- Remote Fault/Local Fault signaling at the Reconciliation Sublayer

We use the AXI4-S bus interface option. Our testing and debug was performed using the unrestricted version of this core.

PCIe Bridge (GEN1/GEN2)
A host interface is required to handle a number of functions related to the TOE128 with configuration being the most important. A PCI bridge is supplied in encrypted net list format (.ncg) for this purpose. The PCIe Bridge has 4-lanes of GEN1/GEN2, and is a full function PCIe core. Configuration, BARs (base address registers), and master-moding DMA engines are included. Drivers with ‘C’ source for Linux are included.

TOE128
The TOE128 implements the TCP function directly in FPGA gates. No external FPGA memory is required. TOE128s can be cascaded to support multiple sessions. The TOE128 IP is intended to be clocked at the standard Ethernet interface frequency of 156.25 MHz, allowing fully synchronous and lowest latency data exchange with the MAC. At 156.25 MHz, the TOE128 operates at the full 10Gbe line rate, generating no Ethernet pause frames. The IP is supplied either as an encrypted .ncg netlist for implementation in Xilinx-based FPGAs or as verilog source to do with as you see fit. Altera Stratix-5 and ASIC versions will follow shortly.