Features

- Hosted via
  - 4-lane GEN1 PCIe (v1.1) via iPASS cable
  - USB2.0
  - 10/100/1000BASE-T Ethernet
  - Stand alone
- Single Xilinx Virtex-7 FPGA:
  - 7V2000T-2,-1 (fastest to slowest)
  - 7VX690T-3,-2,-1
  - 7V585T-3,-2,-1
  - 7VX485T-3,-2,-1
  - 7VX330T-3,-2,-1
- 14+ million ASIC gates (ASIC measure) when stuffed with 7V2000T
- GTP low-powered transceivers (assumes -2 speed grade or faster for 10GbE):
  - 4 SFP+ sockets supports modules for any of the following interfaces:
    - 10 Gigabit Optical Ethernet
      - 10GBase-SR 10GBASE-LR 10GBASE-LRM 10GBase-ER
    - 10 Gigabit Copper Ethernet
      - 10GBASE-R direct attach
    - 10 Gigabit Sonet: 10GBase-LW
    - 10 Gigabit FibreChannel
  - SATA II (device)
  - USB3.0
  - 2 channels using SMA connectors
- Dual, 4-lane PCIe GEN1/GEN2 prototyping via iPASS cable
- Dual SEARAY GTP Expansion headers, 8-lanes each.
  - PCIe
  - CX4
  - 4 SFP+ sockets
  - custom
- 240-pin DDR3 UDIMM
  - 72-bit data width (64-bit with 8-bit ECC)
  - 800 MHz operation, PC3-12800
  - Addressing/power to support 16GB (+ ECC)
  - DDR3 Verilog/VHDL reference design provided (no charge)
  - Optional RLDRAM DIMM instead of DDR3 for ultra low latency
- Alternate pin compatible memory cards available (consult factory for availability):
  - SRAM: QDR, ASYNC, STD, or PSRAM, Flash
  - DRAM: SDR, DDR1, PSRAM or RLDRAM, DDR2
  - Micror, USB PHY, Extra Interconnect
- Marvel MV78200 Discovery Innovation Dual CPU
  - 1 GHz clock
  - Dual USB2.0 ports (Type B connector)
  - Dual Serial-ATA II connectors for 2 external hard drives (SATA II)
  - Gigabit Ethernet interface
  - 10/100/1000 GbE (RJ45 connector)
- Sheeva™ CPU Core (ARM v5TE compliant)
  - Out-of-order execution
  - Single and double-precision IEEE compliant floating point
  - 16-bit Thumb instruction set increases code density
  - DSP instructions boost performance for signal processing applications
  - MMU to support virtual memory features
  - Dual Cache: 32 KB for data and instruction, parity protected
  - L2 cache: 512 KB unified L2 cache per CPU (total of 1MB), ECC protected.
- 1 GB external DDR2 SDRAM
  - Organized in a 128M x 64 configuration
  - 400 MHz (800 MHz data rate with DDR)
- RS232 port for terminal-style observation
- After configuration, both CPUs dedicated entirely to user application
- Linux operating system
  - Source and examples provided via GPL license (no charge)
  - ~15 seconds to CPU boot
- Three independent low-skew global clock networks
  - G0, G1, G2
  - Three, high-resolution, user-programmable synthesizers for G0, G1, G2
  - Silicon Labs Si5326: 2kHz to 945 MHz
  - User configurable via Marvell uP RS232, USB, PCIe, or Ethernet
  - Global clocks networks distributed differentially and balanced
- Flexible customization via 3 daughter cards positions
  - DINARI expansion connector
  - Connector is non-proprietary, readily available, and cheap
  - 72 LVDS pairs + clocks (or 144 single-ended)
  - 700 MHz on all signals with source synchronous LVDS
  - Signal voltage set by daughter card (+xV to +xV)
  - Reset
  - Supplied power rails (fused):
    - +12V (24W max)
    - +3.3V (10W max)
  - Pin multiplexing to/from daughter cards using LVDS (up to 10x)
- Fast and Painless FPGA configuration
  - USB, cabled PCIe, Ethernet, JTAG
  - Stand-alone configuration with USB stick
  - Configuration Error reporting
  - Accelerated configuration readback for advanced debug
- RS232 port for embedded FPGA-based SOC uP debug
  - Accessible from all FPGAs via separate 2-signal bus
- Full support for embedded logic analyzers via JTAG interface
  - ChipScope, Veridae, and other third-party debug solutions
- Status FPGA-controlled LEDs
  - Enough multicolored LEDs to light a fish tank.

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Description

Overview

The **DNV7F1A** is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The **DNV7F1A** is a stand-alone system and can be hosted by 4-lane PCIe cable (GEN1), USB or Ethernet. A single **DNV7F1A** configured with a single Virtex-7, 7V2000T can emulate up to 14 million gates of logic as measured by a reasonable ASIC gate counting standard. This gate count estimate number does not include embedded memories and multipliers resident in the FPGA fabric. One hundred percent (100%) of the Virtex-7 FPGA resources are available to the user application. The **DNV7F1A** achieves high gate density and allows for fast target clock frequencies by utilizing FPGAs from Xilinx's 28nm Virtex-7 family.

**Virtex-7 FPGA from Xilinx**

The **DNV7F1A** uses a high I/O-count, 1761-pin flip-chip BGA package (FFG1761, FLG1761, FHG1761). In this package, the largest device, the 7V2000T, has 850 I/Os. All I/Os are utilized and please note the reduced functionality when this product is stuffed with the 7VX330T or 7VX485T. Abundant fixed interconnects (either differential or single-ended) are provided between the user FPGA and the configuration FPGA. 100% of the resources of the user Virtex-7 FPGA is dedicated to the user application.

The maximum density stuffing option utilizes the 7V2000T. When stuffed with this device, **DNV7F1A** is capable of prototyping &gt;14 million gates of ASIC logic with plenty of resource margin. This is a ground breaking device and the first to utilize 2.5 silicon dimensions. Prior to the stacked 7V2000T, the biggest challenge in FPGA-based ASIC prototyping was logic partitioning. This difficult task is nearly eliminated with this large quad-slice device.

**The Marvell MV78200 Discovery™ Dual CPU**

A MONSTER for data movement and manipulation

Easy FPGA configuration is a required feature of large FPGA boards. We use an onboard CPU to handle this function. We choose a Marvell MV78200 from the Discovery™ Innovation CPU family. Bluntly stated, this CPU is massive, massive overkill for the mundane task of FPGA configuration. The MV78200 comes a variety high performance interfaces, and all can be utilized to your advantage.

**Dual Sheeva™ CPUs, 1GHz with floating point**

First and foremost are dual CPUs. And after we are done configuring the FPGAs we dedicate both CPUs to your application. The CPUs in the MV78200 are Marvell Sheeva™ cores, which are ARM v5TE compliant. The CPUs are clocked at 1GHz and each processor has a single and double precision floating point unit. A fixed 1 GB, DDR2 memory is standard and is useful for large amounts of high speed data buffering. The memory is organized as 128M x 64 and clocked at the full frequency allowed: 400MHz (800 MHz effective with DDR). This DDR2 bank is shared between the two CPUs. Boot code is resident in an SPI Flash, and application code is downloaded via any port: PCIe, USB, and Ethernet. We ship Linux as the standard operating system. Options exist for VxWorks and other real-time operating systems. Contact the factory for more information.

**PCI Express**

The Marvell 78200 acts as a two-port high-speed PCI Express switch (2.5 Gb/s). It connects the user FPGA at 4-lane PCI Express speeds to a host computer. The Marvell 78200 has multiple DMA engines to pump data to and from any port. The user interface on the FPGA is a simple-to-use, pipelined A/D bus running at 6.4Gb/s. Drivers for data movement to and from a host machine are provided. A simple example FPGA design and host computer application streaming data at PCI Express x4 bandwidth to the user FPGA is provided.

**Two Serial-ATA Ports (SATA II)**

The MV78200 has two Serial-ATA Generation 2 (SATA II) ports, each capable of running at 3.0 Gb/s. SATA is intended for high speed data transfer to/from serial-ATA hard drives. Two SATA connectors are provided, allowing for direct, high-speed interfacing to external hard drives. The MV78200 has specialized enhanced DMA (EDMA)
engines for HDD data transfer with 512-byte buffer for each channel. Examples of all possible data movement options, with source, are included.

GbE – 802.3 Gigabit Ethernet
The MV78200 can be controlled over its built-in Ethernet port. The interface is a standard RJ45 connector. This port can be used to configure FPGAs, set board clocks and other resources, and access the Linux terminal. This terminal can also be used to send data to and from the user FPGA design at gigabit Ethernet speeds.

Daughter cards for customization and expansion
The DNV7F1A introduces a new expansion connector standard to our products called DINIARRAY (DINAR1). Three 320-pin Samtec SEAM series connectors are attached to the user FPGA A, enabling expansion and customization with daughter cards. This is a non-proprietary, industry standard connector and the mating connector is readily available. We can provide the mating connector to you at our cost. We are not fans of proprietary, hard-to-get, outrageously priced expansion connectors. The 144 signals (72 pairs) to/from each of these expansion connectors are routed differentially and can run at the limit of the Virtex-7 FPGA I/Os: 710 MHz (assumes -2 or faster). Clocks, resets, and presence detection, along with abundant (fused) power are included in each connector.

Memory
A single PC3-10600 DDR3 UDIMM socket enables up to 16GB (plus ECC) of memory for bulk storage and lookup. With a 16GB UDIMM memory stick, the configuration is 2048M x 72. Using a -1 speed grade V7 FPGA, this interface is tested at the maximum FPGA I/O frequency: 800 MHz (1600 Mb/s with DDR). You are welcome to use this memory as 64-bits with 8 bits of error correction (ECC), or as a 72-bit memory without correction. This is the same UDIMM interface used in our blockbuster DNPCIe_10G_HXT_LL product. We, of course, provide several verilog examples for no charge that you are welcome to use. All functions of the DDR3 DRAM can be exploited and optimized. Up to 8 banks can be open at once. Timing variables such as CAS latency and precharge can be tailored to the minimum given your operating frequency and the timing specification of the exact DDR3 memory utilized. Alternate UDIMM memories are available, including an RLDRAM and a QDRII+ option.

Easy Configuration via PCIe, USB, or Ethernet
Configuration of the FPGAs is under the control of the Marvell CPU. Configuration data can be provided over PCI Express, USB, Ethernet, or on-board non-volatile memory. It can be copied to the board using a USB memory stick (provided). Configuration occurs automatically after the CPU boots. Sanity checks are performed automatically on the configuration files, streamlining the configuration process in the case of human error. Multiple LEDs provide instant status and operational feedback.

Status LEDs, Debug
As with all of our ASIC emulation boards, the DNV7F1A is loaded with LEDs. The LEDs are stuffed in several different colors (red, green, blue, orange et al.). There are enough LEDs here to adequately illuminate a fish tank. When testing this make sure an adult is present and don’t electrocute yourself. These LEDs are user controllable from the FPGAs so can be used as visual feedback in addition the party enhancing. A JTAG connector provides an interface to ChipScope and other third party debug tools.