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# Table of Contents

**INTRODUCTION** ......................................................................................................................... 1

1. **DNV7F2B LOGIC EMULATION KIT** ......................................................................................... 1

2. **DNV7F2B LOGIC EMULATION BOARD FEATURES** ........................................................ 4

3. **PACKAGE CONTENTS** ........................................................................................................... 9

4. **INSPECT THE BOARD** ............................................................................................................ 10

5. **ADDITIONAL INFORMATION** ................................................................................................. 10

**GETTING STARTED** ....................................................................................................................... 11

1.1 **BEFORE YOU BEGIN** ........................................................................................................ 11

1.2 **Warnings** ............................................................................................................................ 11

2. **INSTALLING THE SOFTWARE** ............................................................................................. 12

2.1 **Exploring the Customer Support Package** .......................................................................... 12

3. **BOARD SETUP** ..................................................................................................................... 13

3.1 **Install FPGA Heatsinks** ...................................................................................................... 13

3.2 **Before Powering Up the Board** ......................................................................................... 13

3.3 **Powering Up the Board** ...................................................................................................... 14

4. **RUNNING THE FIELD TEST** ............................................................................................... 15

**PROGRAMMING/CONFIGURING THE HARDWARE** ................................................................... 17

1. **INTRODUCTION** ................................................................................................................... 17

2. **EMU GRAPHICAL USER INTERFACE (GUI)** ....................................................................... 18

3. **CONFIGURING THE VIRTEX-7 FPGAS USING EMU** ...................................................... 19

4. **Before Powering Up the Board** ............................................................................................ 20

4.1 **Setup – Configuring the Virtex-7 FPGAs using JTAG** ...................................................... 21

4.2 **Powering Up the Board** ..................................................................................................... 21

4.3 **Configuring the FPGA** ....................................................................................................... 21

5. **CONFIGURING THE VIRTEX-7 FPGAS USING THE USB FLASH DRIVE** ....................... 25

6. **CONFIGURING THE CONFIGURATION FPGA USING MASTER SPI** ................................ 26

6.1 **Setup – Configuring the Configuration FPGA using Master SPI** .................................... 26

6.2 **Powering Up the Board** ..................................................................................................... 27

7. **MARVELL SERIAL PORT MONITOR** .................................................................................... 28

7.1 **Setup – Marvell Serial Port Monitor** ................................................................................ 28

7.2 **Open Serial Terminal Session** ........................................................................................... 30

7.3 **Powering Up the Board** ..................................................................................................... 31

7.4 **Verify Software Version** .................................................................................................... 31

7.5 **Update the Linux Kernel** ..................................................................................................... 40

**HARDWARE DESCRIPTION** ......................................................................................................... 33

1. **DESCRIPTION** .................................................................................................................... 33

1.1 **Overview** .......................................................................................................................... 33

2. **MARVELL MV78200 CPU** .................................................................................................. 35

2.1 **Overview** .......................................................................................................................... 35

2.2 **Device Bus and Reset Strapping Options** ......................................................................... 36

2.3 **Boot Options** ................................................................................................................... 40

2.3.1 **Booting from SPI Flash** ................................................................................................ 41

2.3.2 **Booting from NAND Flash** .......................................................................................... 41

2.4 **CPU Memory (DDR2)** ....................................................................................................... 42
# Table of Contents

2.5 PCI Express Interface ................................................................. 42

2.5.1 PCI Express Port 0 .................................................................. 42

2.5.2 PCI Express Port 1 .................................................................. 42

2.5.3 PCI Express Clocking .............................................................. 42

2.6 USB Interface ........................................................................... 43

2.7 Gigabit Ethernet Interface .......................................................... 43

2.8 SATA Interface .......................................................................... 43

2.9 UART (RS232) Interface .............................................................. 43

2.10 Real Time Clock ........................................................................ 43

2.11 Temperature Monitor ................................................................. 44

2.12 JTAG Boundary-Scan (JTAG) Interface ...................................... 44

3 CONFIGURATION FPGA (Virtex-6) .................................................. 44

3.1 Overview .................................................................................. 44

3.2 Summary of Virtex-6 FPGA Features ........................................ 45

3.3 FPGA Configuration (Virtex-6) ................................................... 47

3.3.1 Configuration FPGA M[2:0] Select Resistors ....................... 47

3.3.2 SelectMAP via Marvell CPU .................................................. 48

3.3.3 SPI Serial NOR Flash ............................................................ 48

3.3.4 JTAG .................................................................................. 48

3.4 PCI Express Cable Interface ....................................................... 48

3.4.1 Cable Reference Clocking Options ....................................... 49

3.4.2 Cable Present ........................................................................ 50

3.5 SFP+ Interface .......................................................................... 51

3.6 Interconnect – Configuration FPGA to FPGA A/B ...................... 51

3.6.1 Not Main Bus (NMB) ............................................................ 51

4 FPGA A/B (Virtex-7) ................................................................. 52

4.1 Overview .................................................................................. 52

4.2 Summary of 7 Series FPGA Features ....................................... 52

4.3 FPGA Configuration (Virtex-7) ................................................... 53

4.3.1 FPGA A M[2:0] Select Resistors ......................................... 54

4.3.2 SelectMAP via Configuration FPGA .................................... 54

4.3.3 JTAG ................................................................................ 54

4.4 FPGA Interconnect ................................................................. 55

4.4.1 High-speed (LVDS) IO Bus ................................................... 55

4.5 SPI Serial FLASH (512Mbit) ..................................................... 55

4.6 EEPROM ............................................................................... 55

4.7 Backup Battery ....................................................................... 55

4.7.1 Backup Battery Loads .......................................................... 56

4.8 VCCINT Switching Power Supply ............................................ 56

5 CLOCK GENERATION ................................................................. 56

5.1 Clock Methodology ................................................................. 56

5.2 Clock Multipliers (s5) .............................................................. 58

5.2.1 Clock Multiplier – CLK_G0 ................................................ 58

5.2.2 Connections between the FPGAs and Clock Multipliers ........ 58

5.3 Multiplexed Clocks from FPGA CFA/A/B ................................ 59

5.3.1 Multiplexed Clock Circuit .................................................... 59

5.4 PCI Express Reference Clocks ................................................... 59

5.5 QSFP Clock (LVDS) Oscillators ............................................... 59

5.6 Dedicated I/O Delay Oscillators ............................................... 59

5.7 Daughter Card Header Clocks .................................................... 59

5.7.1 DINAR1 ............................................................................. 60

5.7.2 DNSEAM ........................................................................... 60

5.8 Not Main Bus Clock (NMB) ...................................................... 60

5.9 External FPGA Clock (LVDS) Input via SMA (s2) .................... 60

5.9.1 Multiplexed Clock Circuit .................................................... 60

6 RS232 Port ................................................................................ 60

7 TEMPERATURE SENSOR .......................................................... 61

7.1 Temperature Sensor Circuit ...................................................... 61

8 LED INDICATORS ................................................................. 61

8.1 FPGA Status LEDs .............................................................. 61

8.2 Configuration DONE LEDs .................................................. 62

8.3 Ethernet LEDs ...................................................................... 62

8.4 Power Supply Status LEDs .................................................... 62

8.5 USB Cable LED .................................................................... 62

8.6 Miscellaneous LEDs ............................................................... 62
## TABLE OF CONTENTS

9  POWER DISTRIBUTION........................................................................................................................................... 63  
9.1 Stand Alone Operation ........................................................................................................................................... 63  
9.1.1 External Power Connector ................................................................................................................................... 63  
9.2 Power Sequencing and Reset................................................................................................................................... 64  
9.2.1 Power Sequencing ................................................................................................................................................... 64  
9.2.2 Reset Options............................................................................................................................................................. 64  
10 DAUGHTER CARD HEADERS......................................................................................................................................... 64  
10.1 DINARI Daughter Card .............................................................................................................................................. 64  
10.1.1 Daughter Card clocking .......................................................................................................................................... 64  
10.1.2 FPGA to Daughter Card Header IO Connections ................................................................................................. 64  
10.1.3 Daughter Card Header Pin Description ..................................................................................................................... 64  
10.1.4 Insertion/Removal of the Daughter Card ................................................................................................................ 64  
10.2 DNSEAM Daughter Card (GTX Expansion)............................................................................................................. 65  
11 MECHANICAL................................................................................................................................................................. 65  
11.1 Board Dimensions ......................................................................................................................................................... 65  
11.2 Standard Daughter Card Size ................................................................................................................................... 65  
APPENDIX 71  
1 APPENDIX A: CONSTRAINT FILE .................................................................................................................................... 71  
2 ORDERING INFORMATION .............................................................................................................................................. 71
List of Figures

Figure 1 - DNV7F2B Logic Emulation Board.................................................................4
Figure 2 - USB Flash Drive Directory Structure.............................................................12
Figure 3 - EMU Graphical User Interface........................................................................19
Figure 4 - DNV7F2B Logic Emulation Board Block Diagram.......................................34
Figure 5 - PCIE_CPERSTn Signaling with Power Isolation..........................................50
Figure 6 - Clocking Block Diagram..............................................................................57
Figure 7 - Reset Block Diagram.....................................................................................64
List of Tables

Table 1 – USB Flash Drive Directory Contents................................................................................................................................. 12
Table 2 – Virtex-6 Uncompressed Bitstream Length ............................................................................................................................ 26
Table 3 – Reset Strapping Options ...................................................................................................................................................... 36
Table 4 – Miscellaneous LEDs ............................................................................................................................................................ 62
Introduction

This User Manual accompanies the DNV7F2B Logic Emulation Board. This manual will assist in setting up, using, and understanding the hardware aspects of this product. For specific information regarding the Xilinx Virtex-7 parts, please reference the datasheet on the Xilinx website.

1 DNV7F2B LOGIC Emulation Kit

The DNV7F2B is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DNV7F2B is a stand-alone system and can be hosted by 4-lane PCIe cable (GEN1/2), USB or Ethernet. A single DNV7F2B configured with two Virtex-7 7V2000T can emulate up to 28 million gates of logic as measured by a reasonable ASIC gate counting standard. Two DNV7F2B can be linked together, doubling this gate count to 56 million seamlessly. More DNV7F2B can be linked together if the design grows larger. The gate count estimate number does not include embedded memories and multipliers resident in the FPGA fabric. One hundred percent (100%) of the Virtex-7 FPGA resources are available to the user application. The DNV7F2B achieves high gate density and allows for fast target clock frequencies by utilizing FPGAs from Xilinx's 28nm Virtex-7 family.

Virtex-7 FPGA from Xilinx – Stacked Silicon

The DNV7F2B uses a high I/O-count, 1925-pin flip-chip BGA package (FLG1925). In this package, the largest and only device, the 7V2000T, has 1200 I/Os. All I/Os are utilized. Abundant fixed interconnects (either differential or single-ended) are provided between the user FPGA and the configuration FPGA. 100% of the resources of the two Virtex-7 FPGAs are dedicated to the user application. With two 7V2000Ts, the DNV7F2B is capable of prototyping >28 million gates of ASIC logic with plenty of resource margin. This is a ground breaking device and the first to utilize 2.5 silicon dimensions. Prior to the stacked 7V2000T, the biggest challenge in FPGA-based ASIC
prototyping was logic partitioning. This difficult task is dramatically eased with this large quad-slice device.

**Memory**

Memory can be added to the DNV7F2B via the DINAR1 expansion connector using the DINAR1_SODM204 expansion card. Each DINAR1 can host a single DINAR1_SODM204 expansion card, so as many as six of these cards can be used with the DNV7F2B. The DINAR1_SODM204 has a single 204-pin SODIMM socket. Off-the-shelf DDR3 SODIMM modules work fine, allowing you to add up to 8GB of low cost memory in each DINAR1 position. In addition, we have compatible SODIMMs in the following variations: flash, SSRAM, QDR II+, mobile SDRAM, Mictors, USB2.0 PHYs, and more.

**Stacking two boards together**

Two DNV7F2Bs can be stacked together to double the resources, or added to a DNV7F4A. This page here has more detail using the DNV7F2A: Stacking Two DNV7F2A board together. All functionality is seamlessly maintained including the high performance data movement via the NMB busses. When two DNV7F2Bs are stacked, the resulting system can handle at least 56 million ASIC gates. If more DNV7F2Bs are stacked together, the gate count grows accordingly. If you need to stack a large number of DNV7F2Bs, please call in, since additional hardware might be required.

**The Marvell MV78200 Discovery™ Dual CPU**

The Marvell MV78200 provides a number of high-speed interfaces that are available to the user after configuration. The PCI Express interface between the Marvell MV78200 and the Configuration FPGA provides a high-speed data path to the system interface, whether that is USB, Ethernet or PCI Express.

**PCI Express**

The Marvell MV78200 acts as a two-port high-speed PCI Express switch (2.5 Gb/s). It connects the user FPGA at 4-lane PCI Express speeds to a host computer. The Marvell MV78200 has multiple DMA engines to pump data to and from any port. The user interface on the FPGA is a simple-to-use, pipelined A/D bus running at 6.4Gb/s. Drivers for data movement to and from a host machine are provided. A simple example FPGA design and host computer application streaming data at PCI Express x4 bandwidth to the user FPGA is provided.

**Two Serial-ATA Ports (SATA II)**

The MV78200 has two Serial-ATA Generation 2 (SATA II) ports, each capable of running at 3.0 Gb/s. SATA is intended for high speed data transfer to/from serial-ATA hard drives. Two SATA connectors are provided, allowing for direct, high-speed interfacing to external hard drives. The MV78200 has specialized enhanced DMA
(EDMA) engines for HDD data transfer with 512-byte buffer for each channel. Examples of all possible data movement options, with source, are included.

GbE - 802.3 Gigabit Ethernet

The MV78200 can be controlled over its built-in Ethernet port. The interface is a standard RJ45 connector. This port can be used to configure FPGAs, set board clocks and other resources, and access the Linux terminal. This terminal can also be used to send data to and from the user FPGA design at gigabit Ethernet speeds.

Expansion connectors for customization, memory, and stacking

The DNV7F2B uses a connector standard called DINIARRAY (DINAR1), which utilizes 400-pin Samtec SEARAY series connectors. Three of these connectors are attached to the user FPGA, enabling expansion, customization, and stacking. This is a non-proprietary, industry standard connector and the mating connector is readily available. The 150 signals (72 pairs) to/from each of these expansion connectors are routed differentially and can run at the limit of the Virtex-7 FPGA I/Os: 700 MHz (assumes -2 or faster). Clocks, resets, and presence detection, along with abundant (fused) power are included in each connector.

DINAR1 connectors (A1 and B0) and/or (A2 and B2) can be connected using this card to increase FPGA to FPGA interconnect: DINAR1_INTERCON

Easy Configuration via PCIe, USB, or Ethernet

Configuration of the FPGAs is under the control of the Marvell CPU. Configuration data can be provided over PCI Express, USB, Ethernet, or on-board non-volatile memory. This can be copied to the board using a USB memory stick (provided). Configuration occurs automatically after the CPU boots. Sanity checks are performed automatically on the configuration files, streamlining the configuration process in the case of human error. Multiple LEDs provide instant status and operational feedback.

Status LEDs, Debug

As with all of our ASIC emulation boards, the DNV7F2B is populated with numerous LEDs used for monitor/debug applications. A JTAG connector provides an interface to ChipScope, Tektronix Certus and other third party debug tools.
2 DNV7F2B Logic Emulation Board Features

![Image of DNV7F2B Logic Emulation Board]

DNV7F2B Virtex-7 Board features the following:

- Hosted via
  - 4-lane GEN1/2 PCIe via iPASS cable
  - USB2.0
  - 10/100/1000BASE-T Ethernet
  - Stand alone

- Xilinx Virtex-7 FPGAs (FLG1925):
  - XC7V2000T -2,-1 (fastest to slowest)

- 28+ million ASIC gates (ASIC measure) when populated with two 7V2000Ts

- FPGA to FPGA interconnect, Single-ended and LVDS
INTRODUCTION – CHAPTER 1

- 800MHz LVDS Chip-to-Chip (1.6Gb/s)
- Source Synchronous Clocking for LVDS
- LVDS pairs can be used as two single-ended signals at reduced frequency (~225MHz)
- Reference designs for integrated I/O pad ISERDES/OSERDES
- 10x pin multiplexing per LVDS pair

- Yes Main Bus (YMB) – Bus between all FPGAs, also used for seamless stacking
- Not Main Bus (NMB) - Connects User FPGAs via dedicated busses to the Configuration FPGA
  - 40 Signals, LVDS
  - 400 MB/s DMA between FPGAs and Configuration FPGA

- GTX Transceivers (Configuration FPGA)
  - 4-lane iPASS connector for PCIe (GEN1/GEN2)
  - SFP (x1)

- GTX High-speed Interfaces (User FPGAs, -2 speed grade required for 10 GbE):
  - FPGA A
    - 4x SFP+ modules for 10 GbE
    - QSFP+ module for 4x 10 GbE or single 40 GbE
  - FPGA B
    - 4x SFP+ modules for 10 GbE
    - 4-lane iPASS connector for PCIe (GEN1/GEN2)

- DNSEAM_NS GTX Expansion headers, 8-lanes each, one per FPGA, each capable of supporting:
  - 8-lane PCIe (GEN1/GEN2) Consult factory for GEN3
  - 2x CX4 - Ethernet, XAUI, Infiniband
  - 8x SFP+ modules for 10 GbE
  - 2x QSFP+ modules for 40 GbE
  - 8x USB3.0/2.0 (A,AB,B)
  - 8x Serial ATA II (SATA II)
  - 8x SMA

- Clocking Resources (LVDS)
Five, high-resolution, user-programmable, clock synthesizers (G0-G4) utilizing the Si5326

- Dedicated I/O Delay Oscillators
- External FPGA Clock (LVDS) Input via MMCX (x2)
- External FPGA Clock (LVDS) Output via MMCX (x2)
- Multiple clocks from the DINAR1 Daughter Card Headers
- Multiplexed Global clocks from FPGA A/B
- Clock Test Points (x5)
- Oscillators for GTX Transceivers – PCIe, SFP, and QSFP
- PCI Express Reference Clocks

- Memory can be added using DINAR1_SODM204 on any (or all) DINAR1 expansion connector(s):
  - DDR3 (native - up to 8GB)
  - DNSODM204_SSRAM (1.8V version)
  - DNSODM204_QUADMIC (four Mictor connectors)
  - DNSODM204_SE (mobile SDRAM)
  - DNSODM204_USB (USB2.0 PHY)
  - DNSODM204_DDR2_FAST
  - DNSODM204_QDRII+
  - DNSODM204_DDR2_2GB
  - DNSODM204_MICTOR_IO (dual Mictor connectors)

- CPU - Marvel MV78200 Discovery Innovation (Dual)
  - CPU Clocks – up to 1 GHz
  - Dual USB2.0 ports (Type A connector)
  - Single USB2.0 ports (Type B connector)
  - Dual Serial-ATA II (SATA)
  - Gigabit Ethernet Interface
    - 10/100/1000 GbE (RJ45)
  - Sheeva™ CPU Core (ARMv5TE compliant)
    - Out-of-order execution
    - Single and double-precision IEEE compliant floating point
    - 16-bit Thumb instruction set increases code density
- DSP instructions boosts performance for signal processing applications
- MMU to support virtual memory features
- Dual Cache: 32 KB for data and instruction, parity protected
- L2 cache: 512 KB unified L2 cache per CPU (total of 1MB), ECC protected.
  - 1 GB external DDR2 SDRAM
    - 266 MHz (533 MHz data rate)
  - After configuration, both CPUs dedicated to user application. (Note that the second core is not instantiated or used by the Linux installation, and that this CPU does not support SMP Linux)
  - LINUX operating system
    - Source and examples provided via GPL license (no charge)

- Five independent low-skew global clock networks and single fixed clock
  - Five, high-resolution, user-programmable synthesizers for G0-G4
    - Silicon Labs Si5326: 2kHz to 945 MHz
  - User configurable via Marvell uP RS232, USB, PCIe, or Ethernet
  - Global clocks networks distributed differentially and balanced

- Flexible customization via 3 daughter cards positions per FPGA
  - DINAR1 expansion connector
    - Connector is non-proprietary, readily available, and cheap
  - 72 LVDS pairs + clocks (or 150 single-ended)
  - 700 MHz on all signals with source synchronous LVDS
  - Signal voltage set by daughter card (+1.2V to +1.8V)
  - Reset
  - Supplied power rails (fused)
    - +12V (24W max)
    - +3.3V (10W max)
  - Pin multiplexing to/from daughter cards using LVDS (up to 10x)
  - Support FMC, logic analyzer, memory expansion

- Fast and Painless FPGA configuration
  - USB, cabled PCIe, Ethernet, JTAG
- Stand-alone configuration with USB stick
- Configuration Error reporting
- Accelerated configuration readback for advanced debug

- RS232 port for embedded FPGA-based SOC μP debug
  - Accessible from all FPGAs via separate 2-signal bus

- Full support for embedded logic analyzers via JTAG interface
  - ChipScope, Tektronix Certus

- Status FPGA-controlled LEDs
  - Enough LEDs to blind a hamster.
3 Package Contents

Before using the kit or installing the software, be sure to check the contents of the kit and inspect the board to verify that you received all of the items. If any of these items are missing, contact Dini Group before you proceed. The DNV7F2B Logic Emulation Board kit includes the following:

- **DNPCIe CBL GEN2** (x1)
- USB 2.0 Flash Drive 4GB (x2)
- Cable Assembly
  - USB 2.0 Cable (x1)
  - RS232 Serial Cable (DB9), 6ft, F/F (x1)
  - Ethernet Cable (RJ45), 6ft (x1)
  - IPASS PCIE Cable 36P, 2M (x2)
- ATX Power Supply (x1)
- Heatsink (User FPGAs)
  - Alpha FPGA Heatsink (x2)
  - Delta High Speed PWM Fan (x2)
  - Fan Grill (x2)
- Customer Support Package (USB Flash Drive)
  - Daughtercards
  - Documentation
    - Component Datasheets (pdf format)
    - User Manual (pdf format)
    - Schematic (pdf format)
  - FPGA_Reference_Design
    - Virtex-7 Reference Designs (Verilog)
Optional items that support development efforts (not provided):

- Xilinx Vivado Design Suite
- Xilinx Platform Cable USB

4 Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Verify that all components are on the board and appear intact.

5 Additional Information

For additional information, please visit http://www.dinigroup.com/. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

<table>
<thead>
<tr>
<th>Resource</th>
<th>Description/URL</th>
</tr>
</thead>
<tbody>
<tr>
<td>User Manual</td>
<td>This is the main source of technical information. The manual should contain most of the answers to your questions</td>
</tr>
<tr>
<td>Dini Group Web Site</td>
<td>The web page will contain the latest user manual, application notes, FAQ, articles, and any device errata and manual addenda. Please visit and bookmark: <a href="http://www.dinigroup.com">http://www.dinigroup.com</a></td>
</tr>
<tr>
<td>Data Book</td>
<td>Pages from Virtex-7 Datasheets, which contains device-specific information on Xilinx device characteristics</td>
</tr>
<tr>
<td>E-Mail</td>
<td>You may direct questions and feedback to Dini Group using this e-mail address: <a href="mailto:support@dinigroup.com">support@dinigroup.com</a></td>
</tr>
<tr>
<td>Phone Support</td>
<td>Call us at 858.454.3419 during the hours of 8:00am to 5:00pm Pacific Time.</td>
</tr>
<tr>
<td>FAQ</td>
<td>The download section of the web page may contain a document called DNV7F2B Frequently Asked Questions (FAQ). This document is periodically updated with information that may not be in the User’s Manual.</td>
</tr>
</tbody>
</table>
Getting Started

Congratulations on your purchase of the DNV7F2B Logic Emulation Board. This chapter describes how to start using the DNV7F2B Logic Emulation Board.

1 Before You Begin

1.1 Configuring the Programmable Components

The DNV7F2B has been factory tested and pre-programmed to ensure correct operation. The user does not need to alter any jumpers or program anything to see the board work.

1.2 Warnings

- Daughter Card Test Headers (Over Voltage) - The 400-pin daughter card test headers are **NOT** 3.3V tolerant. These signals connect directly with the FPGA IO. Take care when handling the board to avoid touching the components and daughter card connections due to ESD.

- Mechanical Stress – Board stiffeners are provided to reduce mechanical stress; however, inserting and removing Daughter Cards may add additional stress that may cause board failures.

- ESD Warning - The board is sensitive to static electricity, so treat the PCB accordingly. The target markets for this product are engineers that are familiar with FPGAs and circuit boards. However, if needed, the following web page has an excellent tutorial on the “Fundamentals of ESD” for those of you who are new to ESD sensitive products:

  ESD Fundamentals
2 Installing the Software

For complete information regarding the Host Software (EMU) and installation instructions, see the “EMU Software Manual” available on the Customer Support Package (USB Flash Drive).

2.1 Exploring the Customer Support Package

The USB Flash Drive contains the following items, see Figure 2:

![USB Flash Drive Directory Structure](image)

A description of the USB Flash Drive directory contents is listed in Table 1. Please visit the Dini Group website for the most recent revision of these documents.

<table>
<thead>
<tr>
<th>USB Flash Drive Directory Contents</th>
<th>Description of Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Daughtercards</td>
<td>Complete documentation on the DINAR1 and DNSEAM Daughter Cards, including the PCIE Cable Daughter Cards.</td>
</tr>
<tr>
<td>Documentation</td>
<td>Contains the Datasheets, Schematics and User Manual for the board.</td>
</tr>
<tr>
<td>FPGA Reference Designs</td>
<td>Contains the source and compiled programming files for the DNV7F2B reference designs.</td>
</tr>
<tr>
<td>Host Software</td>
<td>Provides the Host Software for the Windows and Linux platforms, including the EMU Software Manual.</td>
</tr>
</tbody>
</table>
3 Board Setup

The instructions in this section explain how to use the DNV7F2B Logic Emulation Board. For the purpose of this demonstration, the DNV7F2B will be configured using the Ethernet interface.

3.1 Install FPGA Heatsinks

Unless the board is shipped in a chassis, the board is shipped without the heatsinks installed, in order to avoid damage to the FPGAs. The heatsinks MUST be installed before powering the board.

1. Apply a pea sized blob of the thermal grease in the center of each FPGA.

2. Align heatsink with the mounting holes on the top of the circuit board. For heatsinks with fans, orient the heatsink to put the cable on the heatsink near the fan heater for the FPGA.

3. Screw the heatsink screws into the PEM nuts that are installed into the board.

   Note: Tighten the screws along one diagonal first, then the other (i.e. first tighten two screws furthest away from each other, then the 2nd pair). This ensures equal pressure distribution across the top of the FPGA.

4. Install the fan power cables into the fan headers provided for each FPGA.

   - FPGA A – J6
   - FPGA B – J2

3.2 Before Powering Up the Board

Powering the board with only the ATX Power (24-Pin) connector could lead to overheating of the ATX wires. All power headers should have the appropriate power cable plugged in. Before powering up the board, prepare the board as follows:

1. Attach the ATX Power Supply connectors to the board as follows (ensure all the power connectors are connected, otherwise the wires may overheat):

   - ATX Main Power Connector (24-Pin) – J5
   - PCI Express Power (6-Pin) – (J4, J10)
   - EPS Power (8-Pin) – (J8) – may not be populated

   Note: On the EPS connector +12V/GND is reversed - Do NOT install the wrong connector!
2. Connect the “Ethernet Cable” to the “CPU ETHERNET” header (J66). Note: In order to be able to access the board over the network, the network must support DHCP.

3. If the kit contains DINAR1_SODM204 Daughter Cards, install the daughter cards in the appropriate header and insert a DDR3 SDRAM SODIMM module.


3.3 Powering Up the Board

1. Power up the board by turning ON the ATX power supply and verify the “POWER GOOD” LEDs (DS27 & DS86 – front panel) is ON indicating the presence of +12V/+5V/+3.3V (located at the bottom-middle of the PCB).

2. Open the “EMU” application and select “Board” followed by “Select Board” (select the “DN0287_DNV7F2B xxxxxxx 192.168.1.76 (Ethernet)” board in the drop-down list that matches the serial number of your board.

3. Verify that the board was correctly identified as a “DN0287_DNV7F2B xxxxxxx” in the window. Note: The serial number will be different.
4 Running the Field Test

Select “Test” followed by “Field Test”. The progress of the tests will be displayed in the EMU log window. The following tests will be executed:

- temperature_test
- clock_field_test
- nmb_blockram_test
- single_intercon_test
- single_intercon_fast
- pup_pdn_pull_test
- lvds_intercon_test
Verify that the all the Field tests PASSED.
Programming/Configuring the Hardware

This chapter details the programming and configuration instructions for the DNV7F2B Logic Emulation Board.

1 Introduction

This section of the User Manual presents different methods to configure the Xilinx Virtex-7 FPGAs:

- **Configuring the Virtex-7 FPGAs using EMU** – using the Graphical User Interface (GUI).

- **Configuring the Virtex-7 FPGAs using JTAG** – using the Xilinx “Platform Cable USB” and JTAG.

- **Configuring the Virtex-7 FPGAs using the USB Flash Drive** – using the USB Flash Drive.

- **Configuring the Configuration FPGA using Master SPI** – using the SPI serial Flash PROM.

- **Updating the Marvell MV78200 Software** – lists the procedure to update the Marvell MV78200 software.

Virtex-7 FPGAs are configured by loading application-specific configuration data - the bitstream - into internal memory. Because the Xilinx FPGA configuration memory is volatile, it must be configured each time it is powered-up. The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes. The following configuration modes are supported:
- Slave SelectMAP (parallel) configuration mode (x8)
- JTAG/Boundary-Scan configuration mode

The configuration modes are explained in detail in Chapter 2, Configuration Interfaces of the UG470 - Virtex-7 Series FPGAs Configuration User Guide. The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0]. In Slave SelectMAP mode, FPGA A and B are independently configured from the Configuration FPGA.

## 2 EMU Graphical User Interface (GUI)

EMU is both an end user application for interacting with Dini Group hardware as well as a development kit for extending EMU’s capabilities and writing custom applications. EMU is designed to interface with any Dini Group board that comes with the Marvell processor, see Figure 3. EMU compiles into both a command-line menu-system program (CMD version) and a graphical interface program (GUI version), supporting all functionality in both versions.

EMU supports Windows and Linux platforms, using the QT windowing package for cross-platform support of native GUI interfaces. QT is freely available from the internet and is required for the GUI versions of EMU. It is recommended to use the QT environment in EMU development, but the CMD version can be built without it, using other standard environments such as GCC and MSVC.
For more information regarding EMU, please reference the “EMU Software Manual” available on the Customer Support Package (USB Flash Drive).

### 3 Configuring the Virtex-7 FPGAs using EMU

This section lists detailed instructions for programming the Xilinx Virtex-7 FPGAs using EMU software application. Before configuring the FPGAs, ensure that the EMU software and the driver software are installed on the host computer. The procedure for configuring each FPGA is the same whether the board is hosted via Ethernet, USB or PCI Express. For the purpose of this example, the Ethernet interface will be demonstrated. Note: The Configuration FPGA must be configured in order to drive the FPGA A and B “CSI_B_14” chips select signals.

Note: This User Manual will not be updated for every revision of the EMU software application, so please be aware of minor differences.
3.1 Before Powering Up the Board

Before powering up the board, prepare the board as follows:

1. Attach the ATX Power Supply connectors to the board as follows (ensure all the power connectors are connected, otherwise the wires may overheat):
   - ATX Main Power Connector (24-Pin) – J5
   - PCI Express Power (6-Pin) – (J4, J10)
   - EPS Power (8-Pin) – (J8) – may not be populated
     
     Note: On the EPS connector +12V/GND is reversed - Do NOT install the wrong connector!

2. Connect the “Ethernet Cable” to the “CPU ETHERNET” header (J66). Note: In order to be able to access the board over the network, the network must support DHCP.

3. If the kit contains DINAR1_SODM204 Daughter Cards, install the daughter cards in the appropriate header and insert a DDR3 SDRAM SODIMM module.


3.2 Powering Up the Board

1. Power up the board by turning ON the ATX power supply and verify the “POWER GOOD” LEDs (DS27 & DS86 – front panel) is ON indicating the presence of +12V/+5V/+3.3V (located at the bottom-middle of the PCB).

2. Open the “EMU” application and select “Board” followed by “Select Board” (select the “DN0287_DNV7F2B xxxxxxx 192.168.1.76 (Ethernet)” board in the drop-down list that matches the serial number of your board.

3. Verify that the board was correctly identified as a “DN0287_DNV7F2B xxxxxxxxx” in the window. Note: The serial number will be different.
4. Right-click on the FPGA to be configured and assign the required bitfile.

5. EMU will perform a sanity check on the bit file and configure the FPGA.
6. Verify that the “FPGA A DONE” blue LED (DS1/DS82 – front panel for FPGA A) is enabled, indicating successful configuration of the FPGA.

4 Configuring the Virtex-7 FPGAs using JTAG

This section lists detailed instructions for programming the Xilinx Virtex-7 FPGAs using iMPACT, Version 14.6 tools. Before configuring the FPGA, ensure that the Xilinx software and the “Xilinx Platform Cable USB” driver software are installed on the host computer. The JTAG/Boundary-Scan configuration interface is always available, regardless of the Mode pin settings. The JTAG/Boundary-Scan configuration mode disables all other configuration modes to prevent conflicts between configuration interfaces.

Note: This User Manual will not be updated for every revision of the Xilinx ISE tools, so please be aware of minor differences.
4.1 Setup - Configuring the Virtex-7 FPGAs using JTAG

Before configuring the FPGAs, ensure the following steps have been completed:

1. Attach the ATX Power Supply connectors to the board as follows (ensure all the power connectors are connected, otherwise the wires may overheat):
   - ATX Main Power Connector (24-Pin) – J5
   - PCI Express Power (6-Pin) – (J4, J10)
   - EPS Power (8-Pin) – (J8) – may not be populated

   Note: On the EPS connector +12V/GND is reversed - Do NOT install the wrong connector!

2. Connect the “Xilinx Platform Cable USB” to the “JTAG FPGA A/B” header (J11).

4.2 Powering Up the Board

Power up the board by turning ON the ATX power supply and verify the “POWER GOOD” LEDs (DS27 & DS86 – front panel) is ON indicating the presence of +12V/+5V/+3.3V (located at the bottom-middle of the PCB).

4.3 Configuring the FPGA

To configure the Xilinx FPGA, perform the following steps:

1. Open iMPACT and create a new default project. Select “Configure devices using Boundary-Scan (JTAG)” from the iMPACT welcome menu.
2. iMPACT will identify FPGA A/B (XC7V2000T) in the JTAG chain. A pop-up window will display “Assign New Configuration File”. Assign new configuration files to the individual FPGAs, or select “Bypass” to bypass the option.

3. On the “Attach SPI or BPI PROM” window, select “No” to continue.
4. Select “Program” from the iMPACT command tool bar: A “Configuration Operation Status” box will appear indicating programming progress.

5. Verify that the “FPGAx_DONE” blue LEDs (i.e. DS1/DS82 – front panel for FPGA A) is enabled, indicating successful configuration of the FPGAs.

5 Configuring the Virtex-7 FPGAs using the USB Flash Drive

For complete information regarding configuring the Virtex-7 FPGAs using the USB Flash Drive, see the “EMU Software Manual” available on the Customer Support Package (USB Flash Drive).
6 Configuring the Configuration FPGA using Master SPI

In Master SPI Serial Flash Mode, the Virtex-6 FPGA configures itself from an on board industry-standard SPI Serial NOR Flash. The board is populated with a Micron, N25Q128A, 128Mbit Serial NOR Flash. Table 2 shows the uncompressed configuration file size for the supported Virtex-6 devices.

<table>
<thead>
<tr>
<th>Device</th>
<th>Data Size (Bits)</th>
<th>PROM/Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC6VLX130T</td>
<td>43,719,776</td>
<td>M25P128</td>
</tr>
<tr>
<td>XC6VLX195T</td>
<td>61,552,736</td>
<td>M25P128</td>
</tr>
<tr>
<td>XC6VLX240T</td>
<td>73,859,552</td>
<td>M25P128</td>
</tr>
<tr>
<td>XC6VLX365T</td>
<td>96,067,808</td>
<td>M25P128</td>
</tr>
</tbody>
</table>

Table 2 – Virtex-6 Uncompressed Bitstream Length

Note: This User Manual will not be updated for every revision of the Xilinx ISE tools, so please be aware of minor differences.

6.1 Setup – Configuring the Configuration FPGA using Master SPI

Before configuring the FPGA, ensure the following steps have been completed:

1. Attach the ATX Power Supply connectors to the board as follows (ensure all the power connectors are connected, otherwise the wires may overheat):
   - ATX Main Power Connector (24-Pin) – J5
   - PCI Express Power (6-Pin) – (J4, J10)
   - EPS Power (8-Pin) – (J8) – may not be populated

      Note: On the EPS connector +12V/GND is reversed - Do NOT install the wrong connector!

2. Connect the “Xilinx Platform Cable USB” to the “JTAG CFPGA” header (J43).

3. Connect the “RS232 Serial Cable” to the “RS232-CPU” header (J67). Open a Terminal Emulator and configure the session as follows:
6.2 Powering Up the Board

1. Power up the board by turning ON the ATX power supply and verify the “POWER GOOD” LEDs (DS27 & DS86 – front panel) is ON indicating the presence of +12V/+5V/+3.3V (located at the bottom-middle of the PCB).

2. During the power-up process, monitor the Terminal Emulator window and press “Enter” when the “Hit any key to stop autoboot:” appears in the window (Note: This prevents contention between the Marvell processor and iMPACT during the SPI Flash programming process).
6.3 Configuring the FPGA

To configure the Xilinx FPGA, perform the following steps:

1. Open iMPACT and create a new default project. Select “Configure devices using Boundary-Scan (JTAG)” from the iMPACT welcome menu.
2. iMPACT will identify FPGA (XC6VLX130T, XC6VLX195T or XC6VLX240T – depending on the build option) in the chain. Assign a new configuration file to the FPGA, or select “Bypass” to bypass the option.

“CUST_CD\DNV7F2B\FPGA_Reference_Designs\Programming_Files\dn0287_dnv7f2b\pcie_config\LX130T\pcie_config.bit”

3. On the “Attach SPI or BPI PROM” window, select “No” to continue.
4. Select “Program” from the iMPACT command tool bar: A “Configuration Operation Status” box will appear indicating programming progress.

5. Verify that the “CFPGA DONE” blue LED (DS76/DS83 – front panel) is enabled, indicating successful configuration of the Configuration FPGA.

7 Marvell Serial Port Monitor

A serial port (RS232) is provided for the user to update U-Boot, the Kernel and Firmware running on the Marvell MV78200 CPU. This section lists detailed instructions for setting up the terminal window and verifying the software version. For more information on updating/programming the Marvell MV78200, see the “EMU Software Manual” available on the Customer Support Package (USB Flash Drive).

Note: Minor changes to this procedure may occur over the life of the product, please contact Dini Group for the latest procedures at support@dinigroup.com.
7.1 Setup – Marvell Serial Port Monitor
Before updating/programming the Marvell MV78200 software, ensure the following steps have been completed:

1. Attach the ATX Power Supply connectors to the board as follows (ensure all the power connectors are connected, otherwise the wires may overheat):
   - ATX Main Power Connector (24-Pin) – J5
   - PCI Express Power (6-Pin) – (J4, J10)
   - EPS Power (8-Pin) – (J8) – may not be populated

   Note: On the EPS connector +12V/GND is reversed - Do NOT install the wrong connector!

7.2 Open Serial Terminal Session
Access to the board is allowed via a Serial Terminal Session (RS232).

1. Connect the “RS232 Serial Cable” to the “RS232 - CPU” header (J67). Open a Terminal Emulator and configure the session as follows:

7.3 Powering Up the Board
Power up the board by turning ON the ATX power supply and verify the “POWER GOOD” LEDs (DS27 & DS86 – front panel) is ON indicating the presence of +12V/+5V/+3.3V (located at the bottom-middle of the PCB).
7.4 Verify Software Version

1. Allow the board to complete the boot sequence and press “Enter”, at the Linux prompt enter:

   ```bash
   sh-3.2# emu_mv -h
   ```

2. The version of software running will be displayed in the terminal window.

7.5 Update the Linux Kernel

For more information on updating/programming the Marvell MV78200, see the “EMU Software Manual” available on the Customer Support Package (USB Flash Drive).
Hardware Description

This chapter describes the hardware features of the DNV7F2B Logic Emulation Board.

1 Description

1.1 Overview
The DNV7F2B is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. A high level block diagram of the DNV7F2B Logic Emulation Board is shown in Figure 4, followed by a brief description of each section.
Figure 4 - DNV7F2B Logic Emulation Board Block Diagram
2 Marvell MV78200 CPU

2.1 Overview

The Marvell MV78200 is a dual-core, high-performance, low-power, highly integrated processor with Marvell’s Sheeva™ ARMv5TE-compliant CPU core. Built on Marvell’s innovative Discovery™ system controller platform, the MV78200 is a complete system-on-chip (SoC) solution. Optimized for low power operation, the MV78200 is ideally suited to a wide range of applications ranging from sophisticated routers, switches and wireless base stations to high-volume laser printers applications.

The MV78200 offers unparalleled integration that makes system design simple and cost efficient. The SoC integrates:

- High-performance dual-issue CPU with Vector Floating Point (VFP) support
- 800 MHz and 1 Ghz operating speed
- 32KB-Instruction and 32KB-Data 4-way, set-associative L1 cache per core
- 512KB unified 8-way, set-associative L2 cache per core
- 40/72-bit high bandwidth DDR2 memory interface (up to 800 MHz data rate)
- Four Gigabit Ethernet MACs with interface options
- Two PCI-Express ports (x4 or Quad x1)
- Three USB 2.0 ports with integrated PHYs
- Two SATA 2.0 ports with integrated PHYs
- Security engine
- Pin-compatible with single-core (MV78100) version.

The innovative, on-chip crossbar architecture with any-to-any connectivity enables concurrent transactions among multiple units that results in high system throughput allowing system designers to create high-performance scalable systems.
2.2 Device Bus and Reset Strapping Options

Internal pull-up/down resistors set the default mode of operation of the Marvell MV87200 CPU. External pull-up/down resistors are required to change the default mode of operation. These signals must remain pulled up or down until SYSRSTn de-assertion (zero hold time in respect to SYSRSTn de-assertion). See Table 3 for the default board configuration.

### Table 3 - Reset Strapping Options

<table>
<thead>
<tr>
<th>Configuration Mode</th>
<th>Configuration Resistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV_D[0] Reserved</td>
<td>R1626 (pull-down)</td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x0.</td>
<td>R617</td>
</tr>
<tr>
<td>DEV_D[1] Reserved</td>
<td>R1627 (pull-down)</td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x0.</td>
<td>R618</td>
</tr>
<tr>
<td>DEV_D[2] PCI Express port0 mode select</td>
<td>R1617 (pull-down)</td>
</tr>
<tr>
<td>*0 = Endpoint</td>
<td>R608</td>
</tr>
<tr>
<td>1 = Root Complex</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled up to 0x1.</td>
<td></td>
</tr>
<tr>
<td>DEV_D[3] PCI Express port0 configuration</td>
<td>R1614 (pull-down)</td>
</tr>
<tr>
<td>*0 = x4</td>
<td>R606</td>
</tr>
</tbody>
</table>
### Configuration Mode

<table>
<thead>
<tr>
<th>Configuration Mode</th>
<th>Configuration Resistors</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DEV_D[4]</strong> PCI Express port1 configuration</td>
<td>R1615 (pull-down)</td>
</tr>
<tr>
<td><em>0 = x4</em></td>
<td>R1616 (pull-down)</td>
</tr>
<tr>
<td>1 = Quad x1</td>
<td>R611 (pull-up)</td>
</tr>
<tr>
<td>NOTE: Internally pulled up to 0x1.</td>
<td>R1600 (pull-down)</td>
</tr>
<tr>
<td><strong>DEV_D[7:5]</strong> HCLK Frequency select</td>
<td>R1601 (pull-down)</td>
</tr>
<tr>
<td>0x0 = 167 MHz</td>
<td>R603 (pull-up)</td>
</tr>
<tr>
<td>0x0 = Reserved</td>
<td>R593 (pull-up)</td>
</tr>
<tr>
<td>0x1 = 200 MHz</td>
<td>R1586 (pull-down)</td>
</tr>
<tr>
<td><em>0x2 = 267 MHz</em></td>
<td>R596 (pull-up)</td>
</tr>
<tr>
<td>0x3 = 333 MHz</td>
<td>R1619 (pull-down)</td>
</tr>
<tr>
<td>0x4 = 400 MHz</td>
<td>R597 (pull-up)</td>
</tr>
<tr>
<td>0x5 = 250 MHz</td>
<td>R1584 (pull-down)</td>
</tr>
<tr>
<td>0x6 = 300 MHz</td>
<td>R595 (pull-up)</td>
</tr>
<tr>
<td>0x7 = Reserved</td>
<td>R1567 (pull-down)</td>
</tr>
<tr>
<td>NOTE: Internally pulled to 0x2.</td>
<td>R594</td>
</tr>
<tr>
<td><strong>DEV_D[11:8]</strong> PCLK0 to HCLK ratio</td>
<td>R1601 (pull-down)</td>
</tr>
<tr>
<td>0x0 = 1</td>
<td>R603 (pull-up)</td>
</tr>
<tr>
<td>0x1 = 1.5</td>
<td>R593 (pull-up)</td>
</tr>
<tr>
<td>0x2 = 2</td>
<td>R1586 (pull-down)</td>
</tr>
<tr>
<td>0x3 = 2.5</td>
<td>R596 (pull-up)</td>
</tr>
<tr>
<td>0x4 = 3</td>
<td>R1619 (pull-down)</td>
</tr>
<tr>
<td>0x5 = 3.5</td>
<td>R597 (pull-up)</td>
</tr>
<tr>
<td><em>0x6 = 4</em></td>
<td>R1584 (pull-down)</td>
</tr>
<tr>
<td>0x7 = 4.5</td>
<td>R595 (pull-up)</td>
</tr>
<tr>
<td>0x8 = 5</td>
<td>R1567 (pull-down)</td>
</tr>
<tr>
<td>0x9 = 5.5</td>
<td></td>
</tr>
<tr>
<td>0xA = 6</td>
<td></td>
</tr>
<tr>
<td>0xB - 0xF = Reserved</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled to 0x4.</td>
<td></td>
</tr>
<tr>
<td><strong>DEV_D[13:12]</strong> CPU0 L2 to PCLK0 ratio</td>
<td>R596 (pull-up)</td>
</tr>
<tr>
<td>0x0 = 1</td>
<td>R1619 (pull-down)</td>
</tr>
<tr>
<td><em>0x1 = 2</em></td>
<td>R593 (pull-up)</td>
</tr>
<tr>
<td>0x2 = 3</td>
<td>R1586 (pull-down)</td>
</tr>
<tr>
<td>0x3 = Reserved</td>
<td>R597 (pull-up)</td>
</tr>
<tr>
<td>NOTE: Internally pulled to 0x1.</td>
<td>R1584 (pull-down)</td>
</tr>
<tr>
<td><strong>DEV_D[17:14]</strong> PCLK1 to HCLK ratio</td>
<td>R595 (pull-up)</td>
</tr>
<tr>
<td>0x0 = 1</td>
<td>R597 (pull-up)</td>
</tr>
<tr>
<td>0x1 = 1.5</td>
<td>R1567 (pull-down)</td>
</tr>
<tr>
<td>0x2 = 2</td>
<td></td>
</tr>
</tbody>
</table>
### Configuration Mode

<table>
<thead>
<tr>
<th>Configuration Mode</th>
<th>Configuration Resistors</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Installed</strong></td>
</tr>
<tr>
<td>0x3 = 2.5</td>
<td></td>
</tr>
<tr>
<td>0x4 = 3</td>
<td></td>
</tr>
<tr>
<td>0x5 = 3.5</td>
<td></td>
</tr>
<tr>
<td><strong>0x6 = 4</strong></td>
<td></td>
</tr>
<tr>
<td>0x7 = 4.5</td>
<td></td>
</tr>
<tr>
<td>0x8 = 5</td>
<td></td>
</tr>
<tr>
<td>0x9 = 5.5</td>
<td></td>
</tr>
<tr>
<td>0xA = 6</td>
<td></td>
</tr>
<tr>
<td>0xB - 0xF = Reserved</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled to 0x4.</td>
<td></td>
</tr>
<tr>
<td>DEV_D[19:18] CPU1 L2 to PCLK1 ratio</td>
<td>R589 (pull-up)</td>
</tr>
<tr>
<td>0x0 = 1</td>
<td>R1573 (pull-down)</td>
</tr>
<tr>
<td><strong>0x1 = 2</strong></td>
<td></td>
</tr>
<tr>
<td>0x2 = 3</td>
<td></td>
</tr>
<tr>
<td>0x3 = Reserved</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled to 0x1.</td>
<td></td>
</tr>
<tr>
<td>DEV_D[20] CPU1 Enable</td>
<td>R1575 (pull-down)</td>
</tr>
<tr>
<td><strong>0 = Disable</strong></td>
<td></td>
</tr>
<tr>
<td>1 = Enable</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x0.</td>
<td></td>
</tr>
<tr>
<td><strong>00 = 8 bits</strong></td>
<td>R1572 (pull-down)</td>
</tr>
<tr>
<td>01 = 16 bits</td>
<td></td>
</tr>
<tr>
<td>10 = 32 bits</td>
<td></td>
</tr>
<tr>
<td>11 = Reserved</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x0.</td>
<td></td>
</tr>
<tr>
<td>DEV_D[24:23] Boot From NAND Flash</td>
<td>R584 (pull-up)</td>
</tr>
<tr>
<td>Defines the default value of bit &lt;NFBoot&gt; in the NAND Flash Control Register</td>
<td>R1565 (pull-down)</td>
</tr>
<tr>
<td>0x0 = Boot from device bus (NOR Flash, ROM ...)</td>
<td></td>
</tr>
<tr>
<td><strong>0x1 = Boot from SPI</strong></td>
<td></td>
</tr>
<tr>
<td>0x2 = Boot from CE don’t care NAND Flash</td>
<td></td>
</tr>
<tr>
<td>0x3 = Boot from CE care NAND Flash</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x0.</td>
<td></td>
</tr>
<tr>
<td>DEV_D[26:25] NAND Flash Initialization Sequence</td>
<td>R1566 (pull-down)</td>
</tr>
<tr>
<td><strong>0x0 = No initialization</strong></td>
<td>R1549 (pull-down)</td>
</tr>
<tr>
<td>0x1 = Init sequence enabled, 3 address cycles</td>
<td></td>
</tr>
<tr>
<td>0x2 = Init sequence enabled, 4 address cycles</td>
<td></td>
</tr>
<tr>
<td>0x3 = Init sequence enabled, 5 address cycles</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x0.</td>
<td></td>
</tr>
<tr>
<td>DEV_D[27] Big Endian initialization</td>
<td>R1550 (pull-down)</td>
</tr>
</tbody>
</table>
**Configuration Mode**

<table>
<thead>
<tr>
<th>Configuration Resistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Installed</td>
</tr>
</tbody>
</table>

*0 = LittleEndian  
1 = BigEndian  
NOTE: Internally pulled down to 0x0.

**DEV_D[28]** CLK25 Select  
0 = Both CLK25_PT and CLK25_SSC are used  
*1 = Only CLK25_PT is used  
NOTE: Internally pulled up to 0x1.

**DEV_D[29]** DRAM Interface Width  
*0 = 64b/72b  
1 = 32b/40b  
NOTE: Internally pulled to 0x0.

**DEV_D[30]** Nand flash initialization command  
*0 = Append command 0x30  
1 = Do not append command 0x30  
NOTE: Internally pulled to 0x0.

**DEV_D[31]** VDDO_C Voltage Select  
*0 = 1.8V  
1 = 3.3V  
NOTE: Internally pulled down to 0x1.

**DEV_ALE[0]** VDDO_B Voltage Select  
*0 = 1.8V  
1 = 3.3V  
NOTE: Internally pulled up to 0x1.

**DEV_ALE[1]** VDDO_D Voltage Select  
*0 = 1.8V  
1 = 3.3V  
NOTE: Internally pulled up to 0x1.

**DEV_WEn[0]** VDD_GE Voltage Select  
*0 = 1.8V  
1 = 3.3V  
NOTE: Internally pulled up to 0x0.

**DEV_WEn[1]** DEV_WEn and DEV_OEn multiplexing option for A[16:15] bits  
*0 - A[16:15] bits are not multiplexed on OE and WE signals.  
1 - A[16:15] bits are multiplexed on OE and WE signals  
NOTE: Internally pulled down to 0x0.

**DEV_WEn[2]** Reserved (ATE)  
NOTE: Internally pulled down to 0x0.

**DEV_WEn[3]** Reserved (TW)  
NOTE: Internally pulled down to 0x0.
### Configuration Mode

<table>
<thead>
<tr>
<th>Configuration Mode</th>
<th>Configuration Resistors</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DEV_A[0]</strong> TCLK Mode Select</td>
<td></td>
</tr>
<tr>
<td>0 = TCLK is driven from TCLK_IN input</td>
<td>R628 (pull- up)</td>
</tr>
<tr>
<td>*1 = TCLK generated internally by TCLK PLL</td>
<td>R1638</td>
</tr>
<tr>
<td>NOTE: Internally pulled up to 0x1.</td>
<td></td>
</tr>
<tr>
<td><strong>DEV_A[2:1]</strong> TCLK frequency select/TCLK De-skew PLL Tune</td>
<td></td>
</tr>
<tr>
<td>If DEV_A[0] is set to 1 - DEV_A[2:1] functions as TCLK frequency select:</td>
<td>R1639 (pull-down)</td>
</tr>
<tr>
<td>*0x0 = 166MHz</td>
<td>R1625 (pull-down)</td>
</tr>
<tr>
<td>0x1 = 200MHz</td>
<td>R630</td>
</tr>
<tr>
<td>0x2, 0x3 = Reserved</td>
<td>R616</td>
</tr>
<tr>
<td>NOTE: Internally pulled to 0x1.</td>
<td></td>
</tr>
<tr>
<td><strong>GE0_TXD[0]</strong> TCLK De-skwer PLL Frequency Band</td>
<td></td>
</tr>
<tr>
<td>Functions as TCLK De-Skewer PLL Frequency band Select. Relevant for De-skew mode only (DEV_A[0] is set to 0)</td>
<td>R1816 (pull-down)</td>
</tr>
<tr>
<td>*0=166 MHz</td>
<td>R1817</td>
</tr>
<tr>
<td>1=200MHz</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x0.</td>
<td></td>
</tr>
<tr>
<td><strong>GE0_TXD[1]</strong> Reserved</td>
<td></td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x1.</td>
<td>R1814 (pull- up)</td>
</tr>
<tr>
<td><strong>GE0_TXD[3:2]</strong> DEV_ALE Mode Select</td>
<td></td>
</tr>
<tr>
<td>*0x0 = Address 2. ALE 1 TCLK cycle</td>
<td>R1818 (pull-down)</td>
</tr>
<tr>
<td>0x1 = Address 3. ALE 2 TCLK cycle</td>
<td>R1812 (pull-down)</td>
</tr>
<tr>
<td>0x2 = Address 4. ALE 3 TCLK cycle</td>
<td>R1819</td>
</tr>
<tr>
<td>0x3 = Reserved</td>
<td>R1813</td>
</tr>
<tr>
<td>NOTE: Internally pulled down to 0x0.</td>
<td></td>
</tr>
</tbody>
</table>

### 2.3 Boot Options

The Marvell MV78200 dual CPU implementation assumes that the CPU0 boots first, completes the proper chip and system configuration settings, and then enables CPU1 boot. Upon reset de-assertion, CPU0 starts its boot from the DEV_CSn. As part of its boot code, CPU0 sets all the MV78200 configuration registers, initializes the DRAM, wakes up the PCI Express link, and sets the different chip interface address map. It also sets the CPU address decoding windows, enabling CPU1 to boot from a different boot device. CPU0 then clears CPU1’s <CPUReset> field in the CPU Control and Status Register, thereby enabling CPU1 to start booting. Two boot options are provided on the DNV7F2B.
2.3.1 Booting from SPI Flash
Device Bus, DEV_AD[24:23] = 0x1 selects the “Boot from SPI” on the Marvell MV78200 CPU. A general purpose SPI interface is provided. The M25P128 (U114), is a 128 Mbit (16M x 8) Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus instructions allowing clock frequency up to 50 MHz (TCLK/4). The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

An enhanced Fast Program/Erase mode is available to speed up operations in factory environment. The device enters this mode whenever the VPPH voltage is applied to the Write Protect/Enhanced Program Supply Voltage pin (W/VPP). The memory is organized as 64 sectors, each containing 1024 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 65536 pages, or 16777216 bytes.

The whole memory can be erased using the Bulk Erase instruction or a sector at a time using the Sector Erase instruction.

The SPI Flash can be programmed by an “In System Programming” programmer e.g DediProg SF100. A programming header is provided on the board, J42.

2.3.2 Booting from NAND Flash
Device Bus, DEV_AD[24:23] = 0x2 selects the “Boot from CE don’t care NAND Flash” on the Marvell MV78200 CPU. The Marvell MV78200 CPU supports booting from NAND Flash when the first block is placed on 00h block address, and is guaranteed to be a valid block with no errors, see MV-S800598-00C - Functional Specifications for more information.

The MT29F4G08ABBDAH4:D (U162) Flash, is a non-volatile Flash memory that uses NAND cell technology. The device is 4 Gbits and operates from a 1.8V voltage supply. The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 Input/Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100,000 cycles. To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC). The device feature a Write Protect pin (pulled high by R1790) that allows performing hardware protection against program and erase operations.

The device features an open-drain Ready/Busy output that can be used to identify if the Program/Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor.

The device has a Chip Enable Don’t Care feature, which allows code to be directly downloaded by the CPU, as Chip Enable transitions during the latency time do not stop the read operation.
The NAND Flash (U162) is connected to the Device Bus on the Marvell CPU.

### 2.4 CPU Memory (DDR2)

The Marvell MV78200 CPU interfaces to four DDR2 SDRAM (128M x 16) devices via a 64-bit bus M_DQ[63..0]. The DDR2 SDRAM (MT47H128M16RT-25E:C) uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the DDR2 SDRAM effectively consists of a single 4n-bit-wide, one clock-cycle data transfer at the internal DRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O balls. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

### 2.5 PCI Express Interface

The Marvell MV78200 has two PCI Express interfaces, Port 0 and Port 1. PCI Express Port 0 is configured as an Endpoint (DEV_AD[2] = 0), while PCI Express Port 1 is always a Root Complex. The PCI Express ports are PCI Express Base 1.1 compliant and run at 2.5GHz allowing for 2Gb/s of bandwidth in each direction. The PCI Express port uses 64-bit addressing, as a master or target. It supports extended PCI Express configuration space, advanced error reporting, power management, L0s and software L1, interrupt emulation message, and error messages. The device also supports P2P bridging (non-transparent bridge) between PEX0 and PEX1 ports, see MV- S800598-00C - Functional Specifications for more information.

#### 2.5.1 PCI Express Port 0

PCI Express Port 0 is always a Endpoint. These are routed as differential traces, AC-coupled, and connected to J60.

#### 2.5.2 PCI Express Port 1

PCI Express Port 1 is always a Root Complex. These are routed as differential traces, AC-coupled, and connected to the Configuration FPGA.

#### 2.5.3 PCI Express Clocking

Refer to the PCI Express Reference Clocks section of this manual.
2.6 USB Interface
The Marvell MV78200 integrates three USB2.0 compliant ports, including integrated PHYs. Each USB 2.0 interface contains a single dual-role controller that can act as a host or a peripheral controller. USB0/1 (J64) is configured as a Host, used during Stand-alone configuration with a USB Flash Drive. USB2 (J63) is configured as a Device and is used during Stand-alone configuration to interface the EMU GUI. The USB ports have a dedicated DMA for data transfer between memory and port.

The USB signals are routed as differential traces and connect to the Marvell MV78200 via common mode filters (T1/T2/T3).

The NUP2201MR6 (D15/D20/D21) transient voltage suppressors are designed to protect the high speed data lines from ESD. The AP2171 (U180) is an integrated high-side power switch optimized for Universal Serial Bus (USB) and other hot-swap applications.

The AP2171 offer current (1.5A) and thermal limiting and short circuit protection as well as controlled rise time and under-voltage lockout functionality.

2.7 Gigabit Ethernet Interface
The Gigabit Ethernet Port (GbE) includes an IEEE802.3 compliant 10/100/1000Mb MAC. The Alaska 88E1318 (U179) Gigabit Ethernet Transceiver is a physical layer device (PHY) between the Marvell MV78200 and the Ethernet connector (J66). The 88E1318 device supports the reduced pin count for GMII (RGMII) for direct connection to the Marvell MV78200.

The J0G-0001NL (J66) is a Gigabit Ethernet single port jack (RJ45) with integrated magnetics and LEDs.

2.8 SATA Interface
Serial ATA is a high-speed serial link replacement for the parallel ATA attachment of mass storage devices. The serial link employed is a high-speed differential layer that utilizes gigabit technology and 8b/10b encoding. The Marvell MV78200 includes two SATA II compliant ports. The device employs the latest SATA II PHY technology, with 3.0Gbps (Gen2i) and backwards compatible with 1.5 Gbps (Gen1i) SATA I. Both TX/RX signal pairs are differentially routed and AC-coupled with 0.1uF capacitors.

The two SATA II ports connect directly to the Marvell MV78200.

2.9 UART (RS232) Interface
See the RS232 Port section in this user manual.

2.10 Real Time Clock
The DS1338 (U160) serial real-time clock (RTC) is a low-power, full binary-coded decimal (BCD) clock/calendar plus 56 bytes of NV SRAM. Address and data are
transferred serially through an I^2C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The RTC is connected to the Two Wire Serial Interface (TWSI) port 1, and mapped to address 0x68h.

The TWSI master starts a transaction by driving a start condition, followed by a 7-bit slave address and a read/write bit indication. The target TWSI slave responds with an acknowledge etc. In addition to the RTC, the CPU Temperature Monitor (U159) and an EEPROM (U163) are connected to the TWSI1 bus, please see schematic for more information.

**2.11 Temperature Monitor**

The MAX1617A is a precise digital thermometer that reports the temperature of both a remote sensor and its own package. The remote sensor is a diode-connected transistor—typically a low-cost, easily mounted 2N3904 NPN type—that replaces conventional thermistors or thermocouples. Remote accuracy is ±3°C for multiple transistor manufacturers, with no calibration needed. The remote channel can also measure the die temperature of other ICs, such as microprocessors, that contain an on-chip, diode-connected transistor. The Marvell MV78200 is connected to a temperature sensor (U159) via the TWSI1 serial bus. This sensor measures is mapped to address 0x4Ch. The maximum recommended operating temperature of the CPU is 85 degrees. When the CPU measures the temperature above 80 degrees, it will immediately RESET the CPU.

The connection is between the Marvell MV78200 and the Temperature Sensor. Note: There is also an optional connection to the Configuration FPGA (U148).

Note: ERRATA – The THERMAL_A and THERMAL_C analog inputs provide unreliable junction temperature indications across the entire condition range.

**2.12 JTAG Boundary-Scan (JTAG) Interface**

The Marvell MV78200 JTAG interface is used for chip boundary scan as well as for CPU cores debugger. The two CPU core TAP controllers are chained (CPU0_TDO is connected to CPU1_TDI; CPU1_TDO is driven on J_TDO pin). J48, the JTAG connector is used to debug the Marvell MV78200.

### 3 Configuration FPGA (Virtex-6)

#### 3.1 Overview

Virtex-6 FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components to enable designers to focus on innovation as soon as their development cycle begins. Using the third-generation ASMBL (Advanced Silicon Modular Block) column based architecture, the Virtex-6 family contains multiple distinct sub-families. This overview covers the devices in the LXT, SXT, and HXT sub-families. Each sub-family contains a different ratio of features to most efficiently address the needs of a wide variety of advanced logic designs.
In addition to the high-performance logic fabric, Virtex-6 FPGAs contain many built-in system-level blocks. These features allow logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 40 nm state-of-the-art copper process technology, Virtex-6 FPGAs are a programmable alternative to custom ASIC technology. Virtex-6 FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, connectivity, and soft microprocessor capabilities. For more information, please reference the Xilinx Virtex-6 documentation.

3.2 Summary of Virtex-6 FPGA Features

- Three sub-families:
  - Virtex-6 LXT FPGAs: High-performance logic with advanced serial connectivity
  - Virtex-6 SXT FPGAs: Highest signal processing capability with advanced serial connectivity
  - Virtex-6 HXT FPGAs: Highest bandwidth serial connectivity

- Compatibility across sub-families
  - LXT and SXT devices are footprint compatible in the same package

- Advanced, high-performance FPGA Logic
  - Real 6-input look-up table (LUT) technology
  - Dual LUT5 (5-input LUT) option
  - LUT/dual flip-flop pair for applications requiring rich register mix
  - Improved routing efficiency
  - 64-bit (or 32 x 2-bit) distributed LUT RAM option
  - SRL32/dual SRL16 with registered outputs option

- Powerful mixed-mode clock managers (MMCM)
  - MMCM blocks provide zero-delay buffering, frequency synthesis, clock-phase shifting, input-jitter filtering, and phase-matched clock division

- 36-Kb block RAM/FIFOs
  - Dual-port RAM blocks
  - Programmable
  - Dual-port widths up to 36 bits
- Simple dual-port widths up to 72 bits
- Enhanced programmable FIFO logic
- Built-in optional error-correction circuitry
- Optionally use each block as two independent 18 Kb blocks

- High-performance parallel SelectIO technology
  - 1.2 to 2.5V I/O operation
  - Source-synchronous interfacing using
  - ChipSync™ technology
  - Digitally controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support with integrated write-leveling capability

- Advanced DSP48E1 slices
  - 25 x 18, two's complement multiplier/accumulator
  - Optional pipelining
  - New optional pre-adder to assist filtering applications
  - Optional bitwise logic functionality
  - Dedicated cascade connections

- Flexible configuration options
  - SPI and Parallel Flash interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Automatic bus width detection

- System Monitor capability on all devices
  - On-chip/off-chip thermal and supply voltage monitoring
  - JTAG access to all monitored quantities

- Integrated interface blocks for PCI Express® designs
  - Designed to the PCI Express Base Specification 2.0
  - Gen1 (2.5 Gb/s) and Gen2 (5 Gb/s) support with GTX transceivers
  - Endpoint and Root Port capable
- x1, x2, x4, or x8 lane support per block
- GTX transceivers: 150 Mb/s to 6.6 Gb/s
- GTH transceivers: 2.488 Gb/s to beyond 11 Gb/s
- Integrated 10/100/1000 Mb/s Ethernet MAC block
  - Supports 1000BASE-X PCS/PMA and SGMII using GTX transceivers
  - Supports MII, GMII, and RGMII using SelectIO technology resources
  - 2500Mb/s support available
- 40 nm copper CMOS process technology
- 1.0V core voltage (-1, -2, -3 speed grades only)
- Lower-power 0.9V core voltage option (-1L speed grade only)
- High signal-integrity flip-chip packaging available in standard or Pb-free package options

### 3.3 FPGA Configuration (Virtex-6)

The Virtex-6 FPGA is configured by loading application-specific configuration data - the bitstream - into internal memory. Because the Xilinx FPGA configuration memory is volatile, it must be configured each time it is powered-up. The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes. The following configuration modes are supported:

- Slave SelectMAP (parallel) configuration mode (x8)
- Master Serial Peripheral Interface (SPI) Flash configuration mode
- JTAG/Boundary-Scan configuration mode

The configuration modes are explained in detail in Chapter 2, Configuration Interfaces of the UG360 - Virtex-6 FPGA Configuration User Guide. The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0]. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or VCC_CONFIG. The mode pins should not be toggled during and after configuration. The configuration/mode pins can also be driven by the Marvell MV78200 CPU in Slave SelectMAP mode.

#### 3.3.1 Configuration FPGA M[2..0] Select Resistors

The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0] configuration pins.
Select the configuration scheme by driving the Configuration FPGA M[2..0] pins either HIGH or LOW.

### 3.3.2 SelectMAP via Marvell CPU

The Marvell MPP bus is connected to the SelectMAP interface on the Configuration FPGA. The SelectMAP configuration interface provides an 8-bit bidirectional data bus interface to the Virtex-6 configuration logic that can be used for both configuration and readback. CCLK is an input to the Configuration FPGA in Slave SelectMAP mode.

### 3.3.3 SPI Serial NOR Flash

In SPI serial Flash mode, M[2:0] = 001., the Virtex-6 FPGA configures itself from an attached industry-standard SPI Serial Flash (N25Q128A). Although SPI is a standard four-wire interface, various available SPI Flash memories use different read commands and protocol. Besides M[2:0], FS[2:0] pins are sampled by the INIT_B rising edge to determine the type of read commands used by SPI Flash.

For Virtex-6 FPGA configurations, the default address always starts from 0.

### 3.3.4 JTAG

Virtex-6 devices support IEEE standards 1149.1 and 1532. IEEE 1532 is a standard for In-System Configuration (ISC), based on the IEEE 1149.1 standard. JTAG is an acronym for the Joint Test Action Group, the technical subcommittee initially responsible for developing the standard. This standard provides a means to ensure the board-level integrity of individual components and the interconnections between them. The IEEE 1149.1 Test Access Port and Boundary-Scan Architecture is commonly referred to as JTAG. JTAG connector (J43) used to download the configuration files to the Configuration FPGA.

### 3.4 PCI Express Cable Interface

One iPass connector (x4), configured for PCI Express (DownStream), is connected to the Configuration FPGA. The PCI Express External Cabling specification establishes a standard method of using PCI Express technology over a cable by defining cable connectors, copper cabling attributes and electrical characteristics, connector retention, identification and labeling. The board conforms to the PCI Express External Cabling Specification Revision 1.0, enabling high data rates (2.5GT/s) between PCI Express subsystems. Standard cables and connectors have been defined for x1, x4, x8, and x16 link widths. Sideband signaling is provided via the cable to attain compatibility with existing silicon and software; this leverages existing software and infrastructure, provides ease-of-use and helps accelerate adoption of the technology. See PCI Express External Cabling Specification Rev 1.0 available from [PCI-SIG](http://www.pcisig.com) for more information.

The PCI Express Cable Connector supports the following Auxiliary signals:

- CREFCLKp/CREFCLKn (required): Low voltage differential cable reference clock.
- CPRSNTn (required): Cable present detect, an active-low signal provided by a Downstream Subsystem to indicate that it's both present and its power is “good” (within tolerance).

- CPERSTn (required): Cable PERST#, an active-low signal, logically equivalent to system PERSTn (platform reset), driven by the Upstream Subsystem.

- CPWRON (required): Cable Power On, an active-high signal provided by an Upstream Subsystem to notify slave-type Downstream Subsystems to turn their main power on or off, used for example to put a slave Subsystem into the S3 power management state.

- SB_RTN (required): The SideBand Return provides a return current path for all single ended sideband signals, allowing for power domain isolation between Subsystems.

- CWAKEn (required): Cable Wake, an active-low signal that is driven by a Downstream Subsystem to re-activate the PCI Express hierarchy’s main power rails and reference clocks. Although optional for Upstream and Downstream Subsystems, all cable assemblies shall include CWAKEn. It is required on any Subsystem that supports wakeup functionality compliant with the specification.

- +3.3 V POWER (optional for connector): Power provisioning to the connector backshell is provided to allow for active signal conditioning components within the cable assembly. A wire shall not be provided within the cable.

- PWR_RTN (optional for connector): Return path optional for +3.3 V power provisioning.

### 3.4.1 Cable Reference Clocking Options

To control jitter, radiated emissions, and crosstalk, and allow for future silicon fabrication process changes, a low voltage swing, current mode, differential clock is specified. Isolated power domains, between the two Subsystems, are maintained through implementation of AC-coupling capacitors at the source. Supplying the cable reference clock is required from an Upstream Subsystem.

- Downstream Device, Clock from remote REFCLK on cable
3.4.2 Cable Present

“Power Good” signaling is accomplished with the following signals: PCIE_CPERSTn / PCIE_CPWRON, for signaling the status of the Upstream Subsystem, and PCIE_CPRSNTn as described within this section. PCIE_CPRSNTn assertion by the Downstream Subsystem is qualified by the power good condition of the Downstream Subsystem, as illustrated in Figure 5. This provides a mechanism for the Upstream Subsystem to determine whether the power is good within the Downstream Subsystem, enable the reference clock, and initiate Link Training.

Opto-couplers (U183, U184) provide power isolation between the Upstream and the Downstream system. Note: PCIE_CPERSTn is an active LOW signal in "To Slave (Upstream)" mode and an active HIGH signal when in “From Host (Downstream)” mode.

Note: In order to use the PCI Express Cable interface on the Configuration FPGA, please contact the Dini Group for a black box NGC file.
### 3.5 SFP+ Interface

The board provides a Small-factor Pluggable (SFP) connector connected to the high-speed transceivers on the Configuration FPGA. SFP is defined as Small Form-Factor Pluggable standard by the SFP MSA and is most commonly used for Gigabit Ethernet or Fiber Channel applications:

**Fibre Channel** is a gigabit speed network technology primarily used for Storage Networking. Fibre Channel is standardized in the T11 Technical Committee of the InterNational Committee for Information Technology Standards (INCITS), an American National Standard Institute (ANSI) accredited standards committee. It started for use primarily in the **supercomputer** field, but has become the standard connection type for **storage area networks** in **enterprise storage**.

**Gigabit Ethernet** (GbE) is a term describing various technologies for implementing Ethernet networking at a nominal rate of one gigabit per second defined by the IEEE 802.3-2005 standard. There are currently four different standards for Gigabit Ethernet using optical fiber, twisted pair cable, or balanced copper cable. The IEEE 802.3z standard included 1000BASE-SX and 1000BASE-LX transmission over multimode and singlemode fiber and the nearly obsolete 1000BASE-CX for transmission over balanced copper cabling.

Note: In order to use the SFP interface on the Configuration FPGA, please contact the Dini Group for a black box NGC file.

### 3.6 Interconnect – Configuration FPGA to FPGA A/B

#### 3.6.1 Not Main Bus (NMB)

A dedicated, point-to-point, high-speed (LVDS) “Not Main Bus” (NMB) bus is provided between the Configuration FPGA and FPGA A and B respectively.
NMB is a LVDS, 10-bit bus (9-data + 1 source-synchronous clock) in each direction with a maximum operating speed of 1.0 Gbps per signal, for a total of 9.0 Gbps in each direction (full-duplex).

In Source Synchronous mode, any of the clock capable pins can be used as the clock signal.

4 FPGA A/B (Virtex-7)

4.1 Overview

Xilinx 7 series FPGAs comprise three new FPGA families that address the complete range of system requirements, ranging from low cost, small form factor, cost-sensitive, high-volume applications to ultra high-end connectivity bandwidth, logic capacity, and signal processing capability for the most demanding high-performance applications. The 7 series devices are the programmable silicon foundation for Targeted Design Platforms that enable designers to focus on innovation from the outset of their development cycle. The 7 series FPGAs include:

- Artix-7 Family: Optimized for lowest cost and power with small form-factor packaging for the highest volume applications.
- Kintex-7 Family: Optimized for best price-performance with a 2X improvement compared to previous generation, enabling a new class of FPGAs.
- Virtex-7 Family: Optimized for highest system performance and capacity with a 2X improvement in system performance. Highest capability devices enabled by stacked silicon interconnect (SSI) technology.

Built on a state-of-the-art, high-performance, low-power (HPL), 28 nm, high-k metal gate (HKMG) process technology, 7 series FPGAs enable an unparalleled increase in system performance with 2.9 Tb/s of I/O bandwidth, 2 million logic cell capacity, and 5.3 TMAC/s DSP, while consuming 50% less power than previous generation devices to offer a fully programmable alternative to ASSPs and ASICs. All 7 series devices share a scalable, optimized fourth-generation Advanced Silicon Modular Block (ASMBL™) column-based architecture that reduces system development and deployment time with simplified design portability.

4.2 Summary of 7 Series FPGA Features

- Advanced high-performance FPGA logic based on real 6-input lookup table (LUT) technology configurable as distributed memory.
- 36 Kb dual-port block RAM with built-in FIFO logic for on-chip data buffering.
- High-performance SelectIO™ technology with support for DDR3 interfaces up to 1,866 Mb/s.
- High-speed serial connectivity with built-in multi-gigabit transceivers from 600 Mb/s to maximum rates of 6.6 Gb/s up to 28.05 Gb/s, offering a special low-power mode, optimized for chip-to-chip interfaces.

- A user configurable analog interface (XADC), incorporating dual 12-bit 1MSPS analog-to-digital converters with on-chip thermal and supply sensors.

- DSP slices with 25 x 18 multiplier, 48-bit accumulator, and pre-adder for high performance filtering, including optimized symmetric coefficient filtering.

- Powerful clock management tiles (CMT), combining phase-locked loop (PLL) and mixed-mode clock manager (MMCM) blocks for high precision and low jitter.

- Integrated block for PCI Express® (PCIe), for up to x8 Gen3 Endpoint and Root Port designs.

- Wide variety of configuration options, including support for commodity memories, 256-bit AES encryption with HMAC/SHA-256 authentication, and built-in SEU detection and correction.

- Low-cost, wire-bond, lidless flip-chip, and high signal integrity flipchip packaging offering easy migration between family members in the same package. All packages available in Pb-free and selected packages in Pb option.

- Designed for high performance and lowest power with 28 nm, HKMG, HPL process, 1.0V core voltage process technology and 0.9V core voltage option for even lower power.

For more information, please reference the Xilinx Virtex-7 documentation.

### 4.3 FPGA Configuration (Virtex-7)

Xilinx 7 series FPGAs are configured by loading application-specific configuration data—a bitstream—into internal memory. 7 series FPGAs can load themselves from an external nonvolatile memory device or they can be configured by an external smart source, such as a microprocessor, DSP processor, microcontroller, PC, or board tester. In any case, there are two general configuration datapaths. The first is the serial datapath that is used to minimize the device pin requirements. The second datapath is the 8-bit, 16-bit, or 32-bit datapath used for higher performance or access (or link) to industry-standard interfaces, ideal for external data sources like processors, or x8- or x16-parallel flash memory.

Like processors and processor peripherals, Xilinx FPGAs can be reprogrammed, in system, on demand, an unlimited number of times.

Since Xilinx FPGA configuration data is stored in CMOS configuration latches (CCLs), it must be reconfigured after it is powered down. The bitstream is loaded each time into
the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes:

- Slave SelectMAP (parallel) configuration mode (x8, x16, and x32)
- JTAG/boundary-scan configuration mode

The configuration modes are explained in detail in Chapter 2, Configuration Interfaces of the UG470 - Virtex-7 Series FPGAs Configuration User Guide. The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0]. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or VCCO_. The mode pins should not be toggled during and after configuration. The mode pins can also be driven by the CPU in Slave SelectMAP mode. The mode pins should not be toggled during and after configuration.

In Slave SelectMAP mode, FPGA A and B are independently configured from the Configuration FPGA. The mode pins can also be driven by the Configuration FPGA (U148) in Slave SelectMAP mode, thus two sets of configuration mode select resistor exists.

4.3.1 FPGA A M[2..0] Select Resistors
The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0] configuration pins.

Select the configuration scheme by driving the Configuration FPGA M[2..0] pins either HIGH or LOW.

4.3.2 SelectMAP via Configuration FPGA
The Configuration FPGA (U148) is connected to the SelectMAP interface on FPGA A (U1) and FPGA B (U2) with a dedicated 8-bit bidirectional data bus. This allows for faster data transfer and independent FPGA configuration during configuration or readback. CCLK is an input in Slave SelectMAP mode.

4.3.3 JTAG
Xilinx 7 series devices support IEEE standard 1149.1, defining Test Access Port (TAP) and boundary-scan architecture respectively. These standards ensure the board-level integrity of individual components and the interconnections between them. In addition to connectivity testing, boundary-scan architecture offers flexibility for vendor-specific instructions, such as configure and verify, which add the capability of loading configuration data directly to FPGAs. Test Access Port and boundary-scan architecture is commonly referred to collectively as JTAG. JTAG connector (J11) is used to download the configuration files to FPGA A/B.
4.4 FPGA Interconnect

4.4.1 High-speed (LVDS) IO Bus

Between FPGA A and B, the interconnect is routed as LVDS pairs to minimize signal integrity issues. Reference the Figure 4 - DNV7F2B Logic Emulation Board Block Diagram and the XDC file for the FPGA pin assignments. Note: This information is also available in the supplied netlist.

4.5 SPI Serial FLASH (512Mbit)

The Spansion S25FL512S device is a flash non-volatile memory. This device connects to a host system (FPGA) via a Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit (Quad I/O or QIO) serial commands. This multiple width interface is called SPI Multi-I/O or MIO. In addition, the FL-S family adds support for Double Data Rate (DDR) read commands for SIO, DIO, and QIO that transfer address and read data on both edges of the clock. The Eclipse architecture features a Page Programming Buffer that allows up to 256 words (512 bytes) to be programmed in one operation, resulting in faster effective programming and erase than prior generation SPI program or erase algorithms.

Executing code directly from flash memory is often called Execute-In-Place or XIP. By using FL-S devices at the higher clock rates supported, with QIO or DDR QIO commands, the instruction read transfer rate can match or exceed traditional parallel interface, asynchronous, NOR flash memories while reducing signal count dramatically.

The S25FL512S product offers high densities coupled with the flexibility and fast performance required by a variety of embedded applications. It is ideal for code shadowing, XIP, and data storage.

4.6 EEPROM

The Atmel AT24C256C provides 262,144-bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 32,768 words of eight bits each. The device’s cascading feature allows up to eight devices to share a common 2-wire bus.

The purpose of this memory is to store information about an integrated network controller (if one is used) such as the MAC address.

4.7 Backup Battery

The encryption key memory cells are volatile and must receive continuous power to retain their contents. During normal operation, these memory cells are powered by the auxiliary voltage input (VCCAUX), although a separate VCCBATT power input is provided for retaining the key when VCCAUX is removed. Because VCCBATT draws very little current (on the order of nanoamperes), a small watch battery is suitable for this supply. (To estimate the battery life, refer to DS183 - Virtex-7 T and XT FPGAs Data Sheet - DC and AC Switching Characteristics.) At less than a 150 nA load, the endurance of
the battery should be limited only by its shelf life. VCCBATT does not draw any current and can be removed while VCCAUX is applied. VCCBATT cannot be used for any purpose other than retaining the encryption keys when VCCAUX is removed.

In addition to supplying the power for FPGAs, the backup battery (BT1) also provides power for the Real Time Clock (U160). Backup Batteries are available Renanta, Lithium Coin Cell, 1.55V 190mAh from Mouser, P/N 614-357-TS.

4.7.1 Backup Battery Loads
The backup battery supplies the backup to FPGA A/B, Configuration FPGA, and the Real Time Clock.

4.8 VCCINT Switching Power Supply
A distributed point of load (POL) power supply topology is implemented utilizing the SIL80C2, a high-performance 80-A rated, non-isolated power module operating from an input voltage range of 4.7 V to 13.8 V. The SIL80C2 requires two resistors to set the output voltage to +1.0V.

5 Clock Generation

5.1 Clock Methodology
The DNV7F2B has a flexible and configurable clocking scheme. Figure 6 is a block diagram showing the clocking resources and connections. All of the “Clock Networks” on the DNV7F2B are routed point-to-point using dedicated LVDS routes. Since LVDS is a low voltage-swing differential signal, using a single ended input buffer in the FPGA will not work. An example Verilog implementation of a differential clock input is given below:

```
IBUFGDS # (.DIFF_TERM("TRUE")) CLK1_IBUFGi (.O(clk1_ibufg),
.I(CLK_G1_FPGAP), .IB(CLK_G1_FPGAN));
```

The pin assignment in the XDC file:

```
set_property PACKAGE_PIN AU26 [get_ports {CLK_G1_FPGAP}]
set_property PACKAGE_PIN AU27 [get_ports {CLK_G1_FPGAN}]
```

All clock networks have a differential test point terminated by a 100R resistor used to measure clock frequency e.g. TP58. The positive side of the differential signal is connected to pin 1 (square) and the negative side is connected to pin 2 (circular) of the test point.
Five, high-resolution, user-programmable, clock synthesizers (G0-G4) utilizing the Si5326

- Clock Multiplier (U91) - CLK_G0
- Clock Multiplier (U93) - CLK_G1
- Clock Multiplier (U95) - CLK_G2
- Clock Multiplier (U97) - CLK_G3
- Clock Multiplier (U99) - CLK_G4

Multiplexed Clocks from FPGA A/B

- PCI Express Reference Clocks
- QSFP Clock (LVDS) Oscillators
- SFP Clock (LVDS) Oscillators
- Dedicated I/O Delay Oscillators
- Daughter Card (DINAR1) Header Clocks
- Not Main Bus Clock (NMB)
- External FPGA Clock (LVDS) Input via MMCX (x2)
- External FPGA Clock (LVDS) Output via MMCX (x2)
5.2 Clock Multipliers (x5)
The Si5326 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. The Si5326 accepts dual clock inputs ranging from 2 kHz to 710 MHz and generates two clock outputs ranging from 2 kHz to 808 MHz. The two outputs are divided down separately from a common source. The device provides virtually any frequency translation combination across this operating range. The Si5326 input clock frequency and clock multiplication ratio are programmable through an I2C or SPI interface (configured for I2C). The Si5326 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Please refer to the “Any-rate Precision Clocks Si5316, Si5322, Si5323, Si5325, Si5326, Si5365, Si5366, Si5367, Si5368 Family Reference Manual” from Silicon Laboratories for the Si5326 for programming information.

5.2.1 Clock Multiplier - CLK_G0
One of the outputs of the Clock Multiplier (U91) is buffered (U67) and distributed as a general reference clock for the FPGAs while the other output is connected to a buffer used to distribute clocks to the DNC cable card. The clock multiplier (U91) can use either oscillator (Y12) or an external clock input (J14/J15) as a reference input. The clock multiplier (U91) must be programmed via the I2C interface. Signal “RST_G0_SYNTHn” is provided to reset the clock multiplier. LED (DS33) indicates a Loss Of Lock (LOL) condition.

Note: Five clock multipliers (U91, U93, U95, U97 and U99) are on the I2C chain, driven from the Configuration FPGA (U148).

Note: Clock network G0 is special, in that the clock buffer (U67) signals are routed to an additional “local” buffer (U58/U55) that provides four low skew clocks to SLR0/1/3 on FPGA A and SLR1/2/3 on FPGA B, thereby reducing the routing delays across the long-lines for system synchronous clocking.

5.2.2 Connections between the FPGAs and Clock Multipliers
All of the “Clock Networks” on the DNV7F2B are routed point-to-point using dedicated differential (LVDS) traces. The arrival times of the clock edges at each FPGA are phase-aligned (length-matched on the PCB) within about 100ps. These clocks are all suitable for synchronous communication among FPGAs.

Note: The maximum, clock frequency with the CDCLVD1204 differential-to-LVDS clock buffers are 800MHz, see datasheet.
5.3 Multiplexed Clocks from FPGA CF/A/B
The SY58038U is a low jitter, low skew, high-speed 8:1 multiplexer with a 1:2 differential fanout buffer. The SY58038U differential input included Micrel's unique 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. Reference the datasheet for internal termination options on each differential input pair. The SY58038U operates from a +2.5V supply voltage. The fully differential architecture and low propagation delay make it ideal for use in high speed multiplexing applications.

5.3.1 Multiplexed Clock Circuit
CLK_G[0..4]_FPGA[A..B]_OUTp/n and CLK_G[0..4]_CFPGA_OUTp/n are LVDS clock outputs from FPGA A/B and the Configuration FPGA that are multiplexed by the SY58038U (U68). This allows the G[0..4] clock networks to be driven by either the Configuration FPGA or FPGA [A..B].

5.4 PCI Express Reference Clocks
The PCI Express clock from the PCI Express Cable connector (J61) drives FPGA B's GTX Transceiver directly via the ICS874003-05 jitter attenuator. The ICS874003-05 is a high performance Differential-to-LVDS Jitter Attenuator designed for use in PCI Express systems.

Note: When the PCI Express core in FPGA B is configured as upstream, then U118 provides a 100MHz clock. A selection of capacitors, that share pads, are provided to physically wire the clock to the correct source/destination, see schematic for more information.

5.5 QSFP Clock (LVDS) Oscillators
Two programmable clock oscillators (Si570), powered from +2.5V, provides a differential reference clock to the GTX Transceivers on FPGA A. The default frequency for these parts is 100 MHz, but they are reprogrammed to 156.25 MHz immediately after startup. Please reference the datasheet for programming information.

5.5.1 GTX Clock Oscillator – GbE/SFP
The differential oscillator (Y5) outputs are AC-coupled to the GTX Transceiver on FPGA A.

The oscillator power supplies are filtered to reduce power supply noise and jitter.

5.6 Dedicated I/O Delay Oscillators
Every HP I/O block contains a programmable absolute delay primitive called IDELAYE2/ODELAYE2. The IODELAY can be connected to an IOLOGICE2/IOSERDESE2 block. IODELAY is a 31-tap, wraparound, delay primitive with a calibrated tap resolution. IODELAY allows incoming/outgoing signals to be delayed on an individual basis. The tap delay resolution is contiguously calibrated.
by the use of an IODELAYCTRL reference clock. The differential oscillator (Y3) outputs is fanned out to FPGA A/B (U1, U2). The default frequency for these parts is 200 MHz. Please reference the datasheet for programming information if a different frequency is needed. The oscillator power supplies are filtered to reduce power supply noise and jitter.

5.7 Daughter Card Header Clocks

5.7.1 DINAR1
Refer to par 10.1 DINAR1 Daughter Card of this manual for more information.

5.7.2 DNSEAM
Refer to par 10.2 DNSEAM Daughter Card (GTX Expansion) of this manual for more information.

5.8 Not Main Bus Clock (NMB)
A dedicated, point-to-point, high-speed (LVDS) “Not Main Bus” (NMB) bus is provided between the Configuration FPGA to FPGA A/B respectively. A source synchronous clock can be instantiated from any of the signals that connects to a clock capable input.

5.9 External FPGA Clock (LVDS) Input via SMA (x2)
The SY58038U is a low jitter, low skew, high-speed 8:1 multiplexer with a 1:2 differential fanout buffer. The SY58038U differential input included Micrel’s unique 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. Reference the datasheet for internal termination options on each differential input pair. The SY58038U operates from a +2.5V supply voltage. The fully differential architecture and low propagation delay make it ideal for use in high speed multiplexing applications. CLK_G[0..4]_MMCX1_INp/n are LVDS clock inputs from MMCX connectors. SMA to MMCX Cable Assemblies are available from Pasternack.

5.9.1 Multiplexed Clock Circuit
CLK_G[0..4]_MMCX1_INp/n are LVDS clock inputs from MMCX connectors that are multiplexed by the SY58038U (U68, U70, U72, U74, and U76) and allow the G0/G1/G2/G3/G4 clock networks to be driven by the respective MMCX channels.

6 RS232 Port
An RS232 serial port is provided on each FPGA. The RS-232 standard specifies output voltage levels between -5V to -15V for logical 1 and +5V to +15V for logical 0. Input must be compatible with voltages in the range of -3V to -15V for logical 1 and +3V to +15V for logical 0. This ensures data bits are read correctly even at maximum cable lengths between DTE and DCE, specified as 50 feet.
The RS-232 standard has two primary modes of operation, Data Terminal Equipment (DTE) and Data Communication Equipment (DCE). These can be thought of as host or PC for DTE and as peripheral for DCE. The DNV7F2B operates in the DCE mode only.

There are two signals attached to the CPU, FPGA A, and FPGAB.

TX and RX provide bi-directional transmission of transmit and receive data. No hardware handshaking is supported.

7 Temperature Sensor

The MAX31785 is a closed-loop multichannel fan controller. Automatic closed-loop fan control saves system power by operating the fans at the lowest possible speeds. Added benefits of slower fan speeds include lower audible noise, longer fan life, and reduced system maintenance. Based on a user-programmable lookup table (LUT), the device automatically adjusts the speeds of the six independent fans based on one or more of the 11 available temperature sensors. Alternately, an external host can manually command the fan speeds and the device automatically adjusts the fan speeds. The device contains a fan-health-diagnostic function to help users predict impending fan failures. The device can also monitor up to six remote voltages.

7.1.1 Temperature Sensor Circuit

The sensor measures the temperature of the FPGA silicon die. The maximum recommended operating temperature of the FPGA is 85 degrees (commercial rating). When the configuration circuitry measures the temperature of any FPGA above 80 degrees, it will immediately de-configure the FPGA, and prevent it from re-configuring.

When the temperature drops below 80, the configuration circuitry will again allow the FPGA to configure.

The FPGAs can safely operate to a maximum of +125°C, but timing is not guaranteed. Use the temperature setting in the ISE Place and Route tool to make timing allowances for operating the FPGA out-of-range. The temperature limit can be disabled by a menu option in the configuration interface.

8 LED Indicators

The board provides various LED’s to indicate that status of the board. The LEDs are turned ON by driving the GATE of the N-MOSFET HIGH.

8.1 FPGA Status LEDs

Numerous LEDs (Green) are provided to the user as a design aid during debugging. The LEDs can be turned ON by driving the corresponding pin HIGH.
8.2 Configuration DONE LEDs
After the FPGAs have received all the configuration data successfully, it releases the DONE pin, which is pulled high by a pull-up resistor. A low-to-high transition on the DONE indicates configuration is complete and initialization of the device can begin. DONE pin drives an N-MOSFET and turns ON a blue LED when the DONE pin goes high. Two LEDs are provided, one placed near the FPGA, and one for the Front Panel.

8.3 Ethernet LEDs
The Gigabit Ethernet Single Port MagJacks (J66) from Pulse contains two LEDs that are controlled by the Ethernet PHY. See the MV-S104224-00B_88E1116R_Datasheet datasheet for more information on driving the LEDs.

8.4 Power Supply Status LEDs
There are many comparators on the board monitoring the CPU/FPGA power supplies. These monitors are setup as simple window comparators to monitor the power supplies and perform the required power-sequencing. When the board is turned on, before anything is configured, there should be no red LEDs and two green LEDs, “POWER GOOD” (DS27 & DS86 – front edge) will turn green, indicating all power supplies are functioning within design parameters. A power fault will be indicated by the respective LED associated with the power supply that is being monitored.

8.5 USB Fault LED
The AP2171 is an integrated high-side power switch optimized for Universal Serial Bus (USB) and other hot-swap applications. The device complies with USB 2.0 and offer current and thermal limiting, including short circuit protection as well as controlled rise time and under-voltage lockout functionality. A 7ms de-glitch capability on the open-drain Flag output prevents false over-current reporting and will turn on LED (DS81) during an over-current condition.

8.6 Miscellaneous LEDs
Table 4 describes the miscellaneous status LEDs and their associated source.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Source</th>
<th>LED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Marvell 78200 CPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SATA0_ACTn_18 (MPP15)</td>
<td>U150-AF21</td>
<td>DS42</td>
</tr>
<tr>
<td>SATA1_ACTn_18 (MPP14)</td>
<td>U150-AA22</td>
<td>DS43</td>
</tr>
<tr>
<td>Clock Multipliers – LOL Indicators</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNTTH_LOL_G0</td>
<td>U118-18</td>
<td>DS23</td>
</tr>
<tr>
<td>SYNTTH_LOL_G1</td>
<td>U120-18</td>
<td>DS24</td>
</tr>
</tbody>
</table>
Signal Name | Source | LED
--- | --- | ---
SYNTH_LOL_G2 | U122-18 | DS25
SYNTH_LOL_G3 | U124-18 | DS26
SYNTH_LOL_G4 | U126-18 | DS27

Front Panel LED

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Source</th>
<th>LED</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED_BICLR_RED</td>
<td>U151-AL9/AF9</td>
<td>DS45</td>
</tr>
<tr>
<td>CFPGA_LED_LOG</td>
<td>U151-V23</td>
<td>DS52 (RED)</td>
</tr>
</tbody>
</table>

9 Power Distribution

The DNV7F2B Logic Emulation Board supports a wide range of technologies, from legacy devices like serial ports, to DDR3 SDRAM, Ethernet Transceivers and GTX Transceivers on the Xilinx FPGAs. This wide range of technologies, including the various FPGA power supplies requires a variety of power supplies. These are provided on the DNV7F2B Logic Emulation Board using a combination of switching and linear power regulators.

9.1 Stand Alone Operation

An external ATX power supply is used to power the board. The external power supply connects to a 24-pin “Mini-Fit” header (J5), Molex P/N 39-29-9242 (rated at 6A/pin). Due to the power consumption at high loads, additional power headers are provided (J4, J10, and J8 – may not be populated).

All power headers should have the appropriate power cable plugged in;

<table>
<thead>
<tr>
<th>Power Header</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATX Main Power Connector (24-Pin)</td>
<td>J5</td>
</tr>
<tr>
<td>EPS Power (8-Pin)</td>
<td>J8</td>
</tr>
<tr>
<td>PCI Express Power (6-Pin)</td>
<td>J4, J10</td>
</tr>
</tbody>
</table>

Note: On EPS Power Headers, +12/GND are reversed! Do not install a different power header in this location, other than EPS!

9.1.1 External Power Connector

This header is fully polarized to prevent reverse connection and is rated for 600VAC at 6A per contact. A reverse-voltage clamp circuit, utilizing a Diode (D9, D10, D14), is provided to protect the +12V supply.

Note: The power headers are not hot-plug able. Do not attach power while power supply is ON.
9.2 Power Sequencing and Reset

9.2.1 Power Sequencing

The power supply sequencing is done in U89 which is connected to the output of the comparators that monitor voltages and the enable pin on the power supplies. Both the Marvell MV78200 CPU and the Virtex-6/7 FPGAs have power-up requirements. Please refer to the datasheet for the requirements.

9.2.2 Reset Options

FPGA A/B can be reset by the Configuration FPGA. Refer to Figure 7 for a block diagram of the reset topology.

![Figure 7 - Reset Block Diagram](image)

The voltage sequencer logic holds the board in reset until all the power supplies passes the voltage requirements. The front-panel “LOG RST” button is used by the Configuration FPGA to generate a logical reset to the code running in the FPGAs. The “SYS RST” button forces a hard reset on all the devices that can be reset, i.e. CPU, GE. In addition, the Configuration FPGA is reset, which cause the user FPGAs A/B to clear.

10 Daughter Card Headers

10.1 DINAR1 Daughter Card

The DNV7F2B board provides three DINAR1 Daughter Cards per FPGA, two located on the top and one located on the bottom of the board. The primary means of interfacing between the FPGAs and external I/O interfaces are through the DINAR1 IO expansion connectors, three provided per FPGA. These are high-speed/high-density, SEARAY 1.27mm (0.050”) pitch connectors, containing 150 single-ended (72 differential) signals. The DINAR1 header provides dedicated LVDS input/output clocks connected to _CC capable pins on the FPGA, VRP/VRN signals, that could be used for interconnect or DCI termination. Power connections including VCCO power,
power sequencing, and a reset signal. Additional signals are provided for Slave Serial configuration. The DINAR1 daughter card is available in a short/long and wide form-factor. For more detailed information regarding the DINAR1 Daughter Card interface, please reference the DINAR1 Interface Specification, available on the Customer Support Package (USB Flash Drive).

10.1.1 Daughter Card clocking
A wide variety of clocking topologies were considered when designing the DINAR1 interface. A list of reasonable clocking methods are listed and diagramed below:

**Manual Phase Alignment** - Use of a PLL inside the FPGA to manually align the phase of a clock sent from the FPGA to a DINAR1 daughter card.

**Source-Synchronous** - Refers to the technique of sourcing a clock along with the data. Specifically, the timing of unidirectional data signals is referenced to a clock sourced by the same device that generates those signals, and not to a global clock. **Source-Synchronous interfaces are the preferred way of clocking a high-speed interface across the DINAR1 connection.**

Repeat this setup in the opposite direction, as long as the hold time on the device on the DINAR1 card is zero or negative. **Source-Synchronous interfaces are the preferred way of clocking a high-speed interface across the DINAR1 connection.**
One drawback of using source-synchronous clocking is the creation of a separate clock-domain at the receiving device, namely the clock-domain of the clock generated by the transmitting device. This clock-domain is often not synchronous to the core clock domain of the receiving device. For proper operation of the received data with other data already present in the device, an additional stage of synchronization logic is required to transfer the received data into the core clock-domain of the receiving device.

**Skewed Clocks** - The I/O on the FPGA can be used on either rising or falling edges of a clock, 180 degrees out of phase with the daughter card. Alternatively invert the clock output to the daughter card. The maximum frequency of the interface when using this method is effectively reduced by half.
Incorrect Clocking Methods

The following are methods that don't work.

**Hold time violation** - The following diagram shows a method that potentially violates hold time on the device on the DINAR1 card.
PLL cascade - When using PLLs in the FPGA, make sure that there is not another PLL anywhere in the feedback loop of the PLL or it will result in an unreliable phase output.

10.1.2 FPGA to Daughter Card Header IO Connections
Refer to the XDC file for the FPGA pin assignments. Note: This information is also available in the supplied netlist.

10.1.3 Daughter Card Header Pin Description

BxSxxP/N_DQx_LCK and BxSxxP/N_DQx_LCK - The daughter card pin-out defines bidirectional differential clock pins. These clock signals are intended to be used as differential clock signals. These signals are routed to clock capable (_MRCC/_SRCC) inputs on the FPGA.

VCCO Power Supply - On the Virtex-7 FPGA, each IO bank has its own VCCO pins. VCCO is determined by the IO standard for that particular IO bank. Since a daughter card will not always be present on a daughter card connector, a VCCO bias generator is used on the mainboard for each daughter card bank to keep the VCCO pin on the FPGA within its recommended operating range. The daughter card drives VCCO to the required level for the particular IO standard. The VCCO impressed by the daughter card needs to satisfy the $V_{IH\text{MAX}}$ of the FPGA on the mainboard. There are three Adjustable Linear Power Supplies for each DINAR1, one per daughter card IO bank. Refer to the datasheet for the LT1963A from Linear Technology on how to adjust the output voltages if required. Install/remove respective jumper on these power supplies in order to change the output voltage between +1.2V and +1.8V.
Power and Reset - The +12V and +3.3V power rails can be supplied by the Daughter Card Headers if the fuses are installed. Each pin on the SEARAY connector is rated to tolerate 1.1A of current without thermal overload.

For a complete description of the additional signals, refer to the DINAR1 Interface Specification, available on the Customer Support Package (USB Flash Drive).

10.1.4 Insertion/Removal of the Daughter Card
Due to the high density SEARAY connectors, the pins on the plug and receptacle of the connectors are very delicate. When plugging in a daughter card, make sure to align the daughter card first before pressing on the connector. Be absolutely certain that both the small and the large keys at the narrow ends of the SEARAY headers line up BEFORE applying pressure to mate the connectors!

Place it down flat, then press down gently.
10.2 DNSEAM Daughter Card (GTX Expansion)
The DNV7F2B board provides one DNSEAM Daughter Card per FPGA, located on the bottom of the board. These are high-speed/high-density, SEARAY 1.27mm (0.050”) pitch connectors, for breaking out GTX transceivers to commonly used connectors types. Available DNSEAM_NS expansion cards include SFP+, SATA, Infiniband, and Samtec BullsEye. Please inquire to sales@dinigroup.com for card availability or if you require a particular high-speed serial interface.

Each connector has on it eight transceivers lanes (RX and TX), 16 SelectIO signals, 4 REFCLK signals, and over 50W of power on +3.3V, +12V, and +1.8V rails. The daughter board is expected to supply the REFCLK signals to the main board; there are four pairs dedicated to this on the DNSEAM_NS interface.

The DNSEAM_NS daughter boards mount to the bottom of the board, and attach to the baseplate which sits between the main board and the daughter board. The photo below shows the location of the two DNSEAM_NS connectors as seen from the bottom of the board, although in this case the baseplate is not attached; if the baseplate were in this photo, the rest of the board would not be visible, only the DNSEAM_NS connectors would be visible through their apertures in the baseplate.

Reference the DNSEAM_NS Interface Specification, available on the Customer Support Package (USB Flash Drive). The specification provides a detailed electrical and mechanical description, including the connector pin-out, signaling levels, routing rules, mechanical requirements, and connector part numbers.

11 Mechanical

11.1 Board Dimensions
The DNV7F2B Logic Emulation Board measures 381mm x 340mm. for more detailed mechanical information, contact support@dinigroup.com.

11.2 Standard Daughter Card Size
Refer to the Specifications for the DINAR1 and DNSEAM_NS for a complete description of the Daughter Card mechanical requirements, available on the Customer Support Package (USB Flash Drive).
Appendix

1 Appendix A: Constraint File

See the Customer Support Package (USB Flash Drive) for the Xilinx User Constraint Files (XDF).

2 Ordering Information

Request quotes by emailing sales@dinigroup.com. For technical questions email support@dinigroup.com.