Product Brief
January 2016
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**Features**

- Single Xilinx Virtex UltraScale FPGA (A2892):
  - VU440-3, -2, -1 (fastest to slowest)
  - 29+ million ASIC gates (ASIC measure)
- Hosted via
  - 4-lane GEN3 PCIe via iPASS cable, USB2.0
  - 10/100/1000BASE-T Ethernet, or stand alone
- DDR4 Memory can be added using **DNBC_SODM204** using 3 DINAR2 expansion connectors
  - DNSODM204_SSRAM1_8V
  - DNSODM204_QUADMIC (four Mictor connectors)
  - DNSODM204_SE (mobile SDRAM)
  - DNSODM204_USB (USB2.0 PHY)
  - DNSODM204_DDR2_FAST
  - DNSODM204_QDRII+
  - DNSODM204_DDR2_2GB
  - DNSODM204_MICTOR_IO (dual Mictor connectors)
- High Speed interfaces:
  - 2 – QSFP+ sockets for 4x 10 GbE or single 40 GbE
  - 8 – SFP+ sockets for 10 GbE
- DNTC (DINI Transceiver Connector), 16-lanes each. Capable of supporting:
  - 16-lane PCIe (GEN1/GEN2/GEN3)
  - 2x CX4 – Ethernet, XAUI, Infiniband
  - 16x SFP+ modules for 10 GbE
  - 4x QSFP+ modules for 40 GbE
  - 16x USB3.0/2.0 (A,AB,B)
  - 16x Serial ATA II (SATA II)
  - 16x SMA
- TMB busses – Preconfigured high speed data movement between field FPGA and Config FPGA
  - 5 GB/s DMA between FPGAs and Config FPGA
- Main Bus (YMB) for bussed interconnect between stacked FPGAs
  - 40 signals, single-ended
- Marvell MV78200 Discovery Innovation Dual CPU (socketed)
  - 1 GHz clock
  - Dual USB2.0 ports (Type B connector)
  - Dual Serial-ATA II connectors for 2 external hard drives (SATA II)
  - Gigabit Ethernet interface
  - 10/100/1000 GbE (RJ45 connector)
  - SheevaTM CPU Core (ARM v5TE compliant)
  - Out-of-order execution
  - Single and double-precision IEEE compliant floating point
  - 16-bit Thumb instruction set increases code density
  - DSP instructions boosts performance for signal processing applications
- **MMU to support virtual memory features**
- Dual Cache: 32 KB for data and instruction, parity protected
- L2 cache: 512 KB unified L2 cache per CPU (total of 1MB), ECC protected.
- 1 GB external DDR2 SDRAM
  - Organized in a 128M x 64 configuration
  - 400 MHz (800 MHz data rate with DDR)
- RS232 port for terminal-style observation
- After configuration, both CPUs dedicated entirely to user application
- Linux operating system
  - Source and examples provided via GPL license (no charge)
  - ~15 seconds to CPU boot
- Five independent low-skew global clock networks and single fixed clock
  - Five, high-resolution, user-programmable synthesizers for G0-G4
  - Silicon Labs Si5326: 2kHz to 945 MHz
  - User configurable via Marvell uP RS232, USB, PCIe, or Ethernet
  - Global clocks networks distributed differentially and balanced
- Flexible customization and stacking via 24 daughter card connectors
  - DNBC (DINI Bank Connector) expansion connector
  - One bank per connector
  - Daughters cards (1 to 12 connectors <banks>)
  - Added FPGA to FPGA interconnect for stacking
  - Connector: non-proprietary; readily available; cheap
  - 24 LVDS pairs + 4 single-ended, + clocks (or 52 single-ended)
  - TBD (800MHz?) on all signals with source synchronous LVDS
  - Signal voltage set by daughter card (+1.2V to +1.8V)
  - Reset
  - Supplied power rails (fused):
    - +12V (24W max), +3.3V (10W max)
  - Pin multiplexing to/from daughter cards using LVDS (up to 10x)
- Noninvasive debug via FPGA register readback: **DN_Readbacker**
- Fast and Painless FPGA configuration
  - USB, cabled PCIe, Ethernet, JTAG
  - Stand-alone configuration with USB stick
  - Configuration Error reporting
  - Accelerated configuration readback for advanced debug
- RS232 port for embedded FPGA-based SOC uP debug
  - Accessible from all FPGAs via separate 2-signal bus
- Full support for embedded logic analyzers via JTAG interface
  - Vivado Logic Analyzer and other third party solutions.
  - **ProtoLink** debug connection to any/all FPGAs with DNBC adapter card: **DNBC_Protolink**
- Status FPGA-controlled LEDs:
  - Enough multicolored LED’s attract ants.

<table>
<thead>
<tr>
<th>Speed Grades (slowest to fastest)</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>Multipliers (27x18)</th>
<th>Memory</th>
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<tbody>
<tr>
<td>Max (100% util) (1000’s)</td>
<td>Practical (60% util) (1000’s)</td>
<td>Blocks (18kbits)</td>
<td>Total (kbits)</td>
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<tr>
<td>VU440</td>
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<td>48,356</td>
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DNVUF1A ASIC Prototyping Engine Featuring Xilinx Dual Virtex UltraScale FPGAs

Block Diagram

- FPGA
- Virtex Ultrascale
- XCVU440
- A2892
- QSFP
- SFP+
- SFP
- 10/100/1000 Phv
- 10/100/1000 baseT
- LCD Header
- MV Serial User JTAG
- USB
- 128M x 64 DDR2
- 128M NAND FLASH Boot
- SATA II (Host) 2x
- SATA
- CPU
- CPU
- DMA (4x)
- Marvell MV78200
- Global Clocks
- Feedback from stacking
- Clocks
- Stacking
- FPGA
- Virtex
- Ultrascale
- XCVU440
- A2892
- YMB
- DNTMB (In)
- DNTMB (Out)
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- Feedback from stacking
- Clocks
- Stacking
Description

Overview

The **DNVUF1A** is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The **DNVUF1A** is a stand-alone system and can be hosted by a 4-lane PCIe cable (GEN3), USB or Ethernet. A single **DNVUF1A** is configured with a single Virtex UltraScale XCVU440 and can emulate up to 29 million gates of logic as measured by a reasonable ASIC gate counting standard. An infinite number of **DNVUF1As** can be linked together extending this gate count number 1 billion or more seamlessly. The gate count estimate number does not include embedded memories and multipliers resident in the FPGA fabric. One hundred percent (100%) of the Virtex UltraScale FPGA resources is available to the user application. The **DNVUF1A** achieves high gate density and allows for fast target clock frequencies by utilizing FPGAs from Xilinx’s 20nm Virtex UltraScale family.

Stacking multiple boards together

An infinite number of **DNVUF1As** can be ganged together to increase the resources. This page here has more detail: ‘Stacking Multiple DNVUF1As boards together’. All functionality is seamlessly maintained including the high performance data movement via the TMB (Transceiver Main Bus). Interconnect between FPGAs on a single board and between boards in a stack can be configured on a bank-by-bank basis via cables on the **DNBC** connectors. Clocks, resets, and configuration are handled seamlessly.

Virtex UltraScale FPGA from Xilinx

The **DNVUF1A** uses a high I/O-count, 2892-pin flip-chip BGA package. In this package the VU440 has 1404 I/Os and 48 GTH channels (16 Gb/s). As many I/O’s as possible are utilized. All FPGA to daughter card interconnect is routed as LVDS, but can be used single-ended at a reduced frequency. 100% of the resources of the two Virtex UltraScale FPGAs is dedicated to the user application.

Introducing the Xilinx Virtex UltraScale VU440. This is the only device that can be stuff on this product. The XCVU440 is available in three speed grade (fastest to slowest): -3, -2, -1. We estimate that the VU440 can prototype >29 million gates of ASIC logic with plenty of resource margin. This is a ground breaking device and the second generation family from Xilinx to utilize 2.5 silicon dimensions. Prior to the stacked-silicon VU440, the biggest challenge in FPGA-based ASIC prototyping was logic partitioning. This difficult task is nearly eliminated with this large 3-slice device.

The Marvell MV78200 Discovery™ Dual CPU

A MONSTER for data movement and manipulation

Easy FPGA configuration is a required feature of large FPGA boards. We use a custom socketed CPU card to handle this
function. We choose a Marvell MV78200 from the Discovery™ Innovation CPU family. Bluntly stated, this CPU is massive, massive overkill for the mundane task of FPGA configuration. The MV78200 comes a variety high performance interfaces, and all can be utilized to your advantage. Look forward to a higher performance CPU card in the near future.

**Dual Sheeva™ CPUs, 1GHz with floating point**

First and foremost are dual CPUs. And after we are done configuring the FPGAs we dedicate both CPUs to your application. The CPUs in the MV78200 are Marvell Sheeva™ cores, which are ARM v5TE compliant. The CPUs are clocked at 1GHz and each processor has a single and double precision floating point unit. A fixed 1 GB, DDR2 memory is standard and is useful for large amounts of high speed data buffering. The memory is organized as 128M x 64 and clocked at the full frequency allowed: 400MHz (800MHz effective with DDR). This DDR2 bank is shared between the two CPUs. Boot code is resident in an SPI Flash, and application code is downloaded via any port: PCIe, USB, and Ethernet. We ship Linux as the standard operating system. Options exist for VxWorks and other real-time operating systems. Contact the factory for more information.

**PCI Express**

The Marvell 78200 acts as a two-port high-speed PCI Express switch (2.5 Gb/s). It connects the user FPGA at 4-lane PCI Express speeds to a host computer. The Marvell 78200 has multiple DMA engines to pump data to and from any port. The user interface on the FPGA is a simple-to-use, pipelined A/D bus running at 6.4Gb/s. Drivers for data movement to and from a host machine are provided. A simple example FPGA design and host computer application streaming data at PCI Express x4 bandwidth to the user FPGA is provided.

**Two Serial-ATA Ports (SATA II)**

The MV78200 has two Serial-ATA Generation 2 (SATA II) ports, each capable of running at 3.0 Gb/s. SATA is intended for high speed data transfer to/from serial-ATA hard drives. Two SATA connectors are provided, allowing for direct, high-speed interfacing to external hard drives. The MV78200 has specialized enhanced DMA (EDMA) engines for HDD data transfer with 512-byte buffer for each channel. Examples of all possible data movement options, with source, are included.

**GbE - 802.3 Gigabit Ethernet**

The MV78200 can be controlled over its built-in Ethernet port. The interface is a standard RJ45 connector. This port can be used to configure FPGAs, set board clocks and other resources, and access the Linux terminal. This terminal can also be used to send data to and from the user FPGA design at gigabit Ethernet speeds.
Bank-Granular Expansion connectors for customization, memory, and stacking

The DNVUF1A uses a connector standard called DNBC (DINI Bank Connector), which utilizes a Samtec SEAM series connectors. Twenty four of these connectors are attached to the FPGA, enabling expansion, customization, and stacking. This is a non-proprietary, industry standard connector from Samtec and the mating connector is readily available. We can provide the mating connector to you at our cost. We are not fans of proprietary, hard-to-get, outrageously priced expansion connectors. Of the 52 signals in the bank, 24 pairs are routed differentially and can run at the limit of the Virtex UltraScale FPGA I/Os: TBD MHz. The remaining 4 signals are routed single-ended. Clocks, resets, and cable/daughter card presence detection, along with abundant (fused) power are included in each connector.

Memory

Memory can be added to the DNVUF1A via the DNBC expansion connector using the DNBC_SODM204 expansion card. Three DNBC connectors can host a single DINAR2_SODM204 expansion card, so as many as twelve of these cards can be used on a single DNVUF1A. The DINAR2_SODM204 has a 204-pin SODIMM socket. Off-the-shelf DDR3 SODIMM modules work fine, allowing you to add up to 8GB of low cost memory in each position. In addition, we have compatible SODIMMs in the following variations: flash, SSRAM, QDR II+, mobile SDRAM, mictors, USB2.0 PHYs, and more. When the specification settles for DDR4, we’ll describe out solution here.

Easy Configuration via PCIe, USB, or Ethernet

Configuration of the FPGAs is under the control of the Marvell CPU. Configuration data can be provided over PCI Express, USB, Ethernet, or on-board non-volatile memory. The configuration files can be copied to the board using a USB memory stick (provided). Configuration occurs automatically after the CPU boots. Sanity checks are performed automatically on the configuration files, streamlining the configuration process in the case of human error. Multiple LEDs provide instant status and operational feedback.

Status LEDs, Debug

As with all of our ASIC emulation boards, the DNVUF1A is loaded with LEDs. The LEDs are stuffed in several different colors (red, green, blue, orange et al.). There are enough LEDs here to attract ants. Please don’t do this without adult supervision. These LEDs are user controllable from the FPGAs so can be used as visual feedback in addition to collecting insects. A JTAG connector provides an interface to Vivado Integrated Logic Analyzer (ILA) and other third party debug tools. A DNBC daughter card enables a ProtoLink™ interface.