The DNMEG_DVI-200 and DNMEG_DVI-400 provide dual-link input and dual-link output Digital Video Interface (DVI) functionality.

2 Receive Channels of Dual-Link DVI

The receiver channels utilize the Silicon Image SiI163B PanelLink Receiver chip. The SiL163B is DVI1.0 compliant. All 48-bits of the digital interface, along with associated control, is connected to a Xilinx Virtex-4 FX FPGA.

2 Transmit Channels of Dual-Link DVI

The transmit channels utilize the Silicon Image SiL178 (for the 200-pin version) or the SiL1178 (for the 400-pin version). The SiL178 supports single link resolutions of VGA to UXGA resolution (25 - 165Mpps) and dual link resolutions of up to QUXGA (330Mpps). Configuration of the SiL1178 is accomplish using an I2C bus connected to the FPGA, and controlled, usually, by one of the PowerPC’s resident in the FX FPGA. Example verilog/VHDL, and ‘C’ is provided.

Description

The DNMEG_DVI-200 and DNMEG_DVI-400 provide dual-link input and dual-link output Digital Video Interface (DVI) functionality.
**Xilinx Virtex-4 FX FPGA**

The DNMEG_DVI achieves high gate density and allows for fast target clock frequencies by utilizing an FPGA from Xilinx's Virtex-4 FX family for logic and memory. A high I/O-count, 1152-pin, flip-chip BGA is employed, providing for abundant flip-flops and logic. XST synthesis scripts are provided, so no third party tools are needed – just Foundation from Xilinx.

**DDR2 Memory and other features**

A DDR2 SODIMM socket connects to the FPGA and works with off-the-shelf memory modules. At present, 2GB SODIMM’s are readily available and the price is reasonable. We have alternative SODIMM’s if you want to prototype other forms of memory. The list includes RLDRAM, FLASH, SSRAM, QDR SSRAM, SDRAM, DDR1, and others. If you want to debug using an old-fashioned logic analyzer, we have an SODIMM that has micros. An RS232 port allows processor-based visibility, but requires UART logic in the FPGA. Working examples are shipped with the board. A JTAG port allows for ChipScope debug. Other third party tools debug use JTAG.

**RocketI/O**

8 (5 for DNMEG_DVI-400) channels of RocketI/O are connected to SMA’s, allowing for very high-speed interconnection rates. On the DNMEG_DVI-400, an SFP socket has been added, enabling a wide selection of standard serial interfaces.

**Hosted or Stand-Alone**

The DNMEG_DVI-200 is intended to daughter to our ASIC emulation products that use the FCI-Berg 200-pin connector. The DNMEG_DVI-400 is intended to daughter to our ASIC emulation products that use the FCI MEG Array 400-pin connector. Either board can be used stand-alone with an off-the-shelf ATX power supply.

**Debug LED’s**

Ten LED’s are available for debug and any other application the user sees fit. We use the LED’s here in La Jolla to tan Burt, a large male African ostrich (Struthio camelus).

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Speed Grades (slowest to fastest)</th>
<th>Slices or LE’s</th>
<th>FF’s</th>
<th>Gate Estimate</th>
<th>PowerPC Blocks</th>
<th>Memory</th>
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<td>FX</td>
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<tr>
<td>FX60</td>
<td>-10,-11,-12</td>
<td>25,280</td>
<td>50,560</td>
<td>710</td>
<td>10</td>
<td>2</td>
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<tr>
<td>FX100</td>
<td>-10,-11,-12</td>
<td>42,176</td>
<td>84,352</td>
<td>1,180</td>
<td>10</td>
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The following table provides a summary of the FPGA and memory specifications for the DNMEG_DVI-400.

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<thead>
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</tr>
</tbody>
</table>

- **Max I/O’s**
- **FF’s in IO pad**
- **Multipliers (18x18)**
- **PowerPC Blocks**
- **Memory**

Notes:
- Max (100% util) (1000s)
- Practical (60% util) (1000s)
- Total (kbytes)
- Total (kbits)
DNMEG_DVI-400

top

bottom
DNMEG_DVI-200

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