User Manual

DNPCIEXT-S3
DNPCIEXT-S5

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1 Overview

The DNPCIEXT-S3/5 PCI extender is an active PCI bridge extender based on Intel’s 21154 PCI-to-PCI bridge. It allows up to three PCI devices to access the host PCI bus and is intended to make debugging PCI devices as convenient as possible. The extender can be installed in any PCI 2.1 and above compliant host system with 32-bit or 64-bit bus widths, +3.3V or +5V signaling, and 33MHz or 66MHz bus frequencies. Secondary devices installed on the extender may be 32-bit or 64-bit and 33MHz or 66MHz, but signaling voltage is dependent on the extender version (DNPCIEXT-S3 is +3.3V only, DNPCIEXT-S5 is +5V only).

An array of LED’s is provided for convenient observation of many signals. There are a total of nineteen LEDs which give the user information relating to PCI bus activity, primary/secondary voltage, primary/secondary bus frequencies, PCI signals, and power rails.

The extender is capable of slowing the secondary bus to half the primary bus frequency.

The mechanical design of the connectors is intended to prevent plugging a +5V signaling card into a +3.3V slot and to prevent plugging a +3.3V card into a +5V slot. A universal card can go into either type of slot.

CAUTION Do not try to force a device into a slot that is keyed not to accept it. Similarly do not try to mechanically modify a device or slot to accept a device that was not keyed to be accepted.

A combination of the DNPCIEXT-S3 and DNPCIEXT-S5 should be able to handle any known +3.3V to +5V signaling conversion issues.

1.1 Features

The DNPCIEXT-S3/5 64-bit, 66MHz Active PCI Extender includes the following features:

- Active PCI Extender PWB with three 32/64-bit slots
- PCI frequencies up to 66 MHz
- Universal 64-bit PCI connector on primary supports any of the following PCI bus configurations:
- +3.3V, 32/64-bit
- +5V, 32/64-bit

• Fully compliant to the PCI Local Bus Specification, Revision 2.1 or higher
• Intel 21154 PCI-to-PCI Bridge
• +3.3V Regulator provides up to 10A local power to secondary PCI slots (+3.3V is not needed on backplane!)
• LEDs provided for quick system status:
  - +3.3V, +5V, +12V, -12V, VAUX, RST*
  - 66MHz (primary), 66MHz (secondary)
  - Primary PCI I/O Voltage +3.3V/+5V
  - Secondary PCI I/O Voltage +3.3V/5V
  - PCI bus activity (5 LEDs)

Figure 1. provides a block diagram of board operation. Figure 2 shows the locations of key controls and indicators.
Figure 1. DNPCIEXT-S3/5 Board Operation

Primary PCI
32/64-bit 0-66MHz
Universal Connector
+5V or +3.3V

Secondary PCI
Slot0
Slot1
Slot2
32/64-bit, 33/66MHz PCI
32/64-bit, 33/66MHz PCI
32/64-bit, 33/66MHz PCI

All Secondary slots must have
the same I/O voltage! Part
numbers for different I/O
voltage options:
+3.3V I/O - DNPCIEXT-S3
+5.0V I/O - DNPCIEXT-S5

+3.3V / +5V Primary PCI
I/O (VIO)
Detector

+3.3V / +5V Primary PCI
I/O (VIO)

+5V

+3.3V

Jumper

Polyswitch Fuse: 2.6 Amps
or
Fuse: 5.0 Amps

XC9572XL
CPLD

LED[3:0]
PCI Bus Activity

+3.3V / +5V Primary PCI
I/O (VIO)

+12V -12V

rst*

Primary PCI Voltage
I/O (VIO) +3.3V

Secondary PCI Voltage I/O (VIO) +3.3V

Primary PCI Voltage
I/O (VIO) +5.0V

Secondary PCI Voltage I/O (VIO) +5.0V

Regulator 3.3V 5A
Regulator 3.3V 5A

21154
PCI-to - PCI
Bridge

21154 PCI-to - PCI Bridge

PCI-to-PCI Bridge

+5V or +3.3V

VAUX

PVAUX

DIP Switch (3)

Jumper

Test Headers

Primary PCI 66MHz
Secondary PCI 66MHz
Secondary PCI Voltage I/O (VIO) +3.3V
Secondary PCI Voltage I/O (VIO) +5.0V

Primary PCI 66MHz

DIP Switch (3)

Jumper

Primary PCI Voltage I/O (VIO) +3.3V
Primary PCI Voltage I/O (VIO) +5.0V

XC9572XL CPLD

LED[3:0]
PCI Bus Activity

+3.3VP
Regulator 3.3V 5A

32/64-bit, 33/66MHz PCI

Slot0

Slot1

Slot2

32/64-bit, 33/66MHz PCI

32/64-bit, 33/66MHz PCI

32/64-bit, 33/66MHz PCI

+3.3VP

Regulator 3.3V 5A

Jumper

+3.3V

PVAUX

DIP Switch (3)

CFG2[0]

+5V

+3.3V

PCIEXt-S3
PCIEXt-S5

DIP Switch (3)

CFG[2:0]

+3.3V / +5V

Primary PCI Voltage I/O (VIO)

All Secondary slots must have
the same I/O voltage! Part
numbers for different I/O
voltage options:
+3.3V I/O - DNPCIEXT-S3
+5.0V I/O - DNPCIEXT-S5
Figure 2. Location of Key Controls and Indicators
2 Controls and Indicators

2.1 LEDs for System Monitoring

The DNPCIEXT-S3/5 board is provided with DIP switches to adjust voltage configurations and LEDs to help monitor operation and configuration. See Figure 2, for locations of key board elements.

The DNPCIEXT-S3/5 has a total of nineteen LEDs allowing the user to quickly determine the status of the system without the need of an oscilloscope or logic analyzer. Figure 2, shows most of the key control and indicator functions and locations. These nineteen LEDs are grouped into the following five categories (with noted sections for each):

- bus activity (Section 2.1.1)
- primary/secondary power (Section 2.1.2)
- primary/secondary bus frequency (Section 2.1.3)
- PCI signals (Section 2.1.4)
- power rails (Section 2.1.5)

2.1.1 Bus Activity LEDs

Four of the nineteen LEDs are dedicated to different types of bus activity and different sets of PCI bus activity observations. DIP switch 1 (SW1) is used to select among different sets of bus activity that can be displayed on these four LEDs. Refer to Table 1, for a summary of the various switch settings for SW1.

Figure 3, provides a circuit diagram of the LED control. Any detected activity is latched for approximately 8 milliseconds. If a bus operation is observed more frequently than once every 8ms, it is possible for an LED to be continuously illuminated. These switches have no impact on the operation of the PCI buses.

Figure 3. DIP Switch 1 (SW1) Circuitry
Table 1. SW1 Settings and Bus Activity LED Functions

<table>
<thead>
<tr>
<th>LED(0)</th>
<th>LED(1)</th>
<th>LED(2)</th>
<th>LED(3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI bus activity</td>
<td>64-bit operation acknowledged (ACK64-active)</td>
<td>64-bit operation requested (REQ64-active)</td>
<td>PERR- or SERR- occurred</td>
</tr>
<tr>
<td>on</td>
<td>on</td>
<td>on</td>
<td>on</td>
</tr>
<tr>
<td>on</td>
<td>on</td>
<td>on</td>
<td>off</td>
</tr>
<tr>
<td>on</td>
<td>on</td>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>on</td>
<td>off</td>
<td>on</td>
<td>off</td>
</tr>
<tr>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>SLOTO is mastering (GNT[0] is active)</td>
<td>SLOT1 is mastering (GNT[1]* is active)</td>
<td>SLOT2 is mastering (GNT[2]* is active)</td>
<td>FRAME is active</td>
</tr>
<tr>
<td>on</td>
<td>on</td>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>FRAME-followed by TRDY- (completed PCI data transfers)</td>
<td>PCI reads (FRAME- and C/BE[0]-)</td>
<td>PCI write (FRAME- and C/BE[0]+)</td>
<td>STOP-activity</td>
</tr>
<tr>
<td>on</td>
<td>off</td>
<td>on</td>
<td>off</td>
</tr>
<tr>
<td>21154 GP10[0]</td>
<td>21154 GP10[1]</td>
<td>PCI write (FRAME- and C/BE[0]+)</td>
<td>STOP-activity</td>
</tr>
<tr>
<td>All other combinations</td>
<td>undefined</td>
<td>undefined</td>
<td>undefined</td>
</tr>
</tbody>
</table>

PCI Bus Activity - When set to monitor PCI bus activity, LED 0 will light when any of the following signals are active: FRAME-, IRDY-, REQ[0]-, REQ[1]-, or REQ[2]-.

64-bit operations acknowledged - When set to monitor 64-bit operations, LED1 will light when the signal ACK64- has been active, indicating 64-bit transfers have occurred on the secondary bus.

64-bit operations requested - When set to monitor 64-bit operations, LED2 will light when the signal REQ64- has been active. This indicates that 64-bit transfers have been requested on the secondary bus. If the 64-bit transfers are occurring, both LED1 and LED2 will be lit. If LED2 is illuminated and LED1 is not, then 64-bit operations are being requested but the transfers are broken in to 32-bit chunks.

NOTE: These switch settings may be changed at any time.

2.1.2 Primary and Secondary Power LEDs

2.1.2.1 Primary I/O Signaling Voltage

The DNPCIEXT-S3/5 is a universal card. This means that it can be plugged into any known PCI connector. The signaling environment for the primary PCI bus can be either +5V or +3.3V. The DNPCIEXT-S3/5 is automatically configured to the correct I/O
2.1.2.2 Blinking LEDs

If the I/O voltage for the primary bus is not high enough, then the LEDs PVIO +5V and PVIO +3.3V will blink at the same time. There are two comparators on the board to determine the current primary I/O voltage level. Although unlikely, should these LEDs blink alternately, a serious error condition has developed. The comparator for +5V has triggered but the comparator for +3.3V has not. Contact the DINI Group immediately.

2.1.2.3 Secondary I/O Signaling Voltage (SVIO)

The signaling voltage of the secondary bus is indicated by the corresponding active LED. The DNPCIEXT-S3 will have “SVIO +3.3V” on (amber): the DNPCIEXT-S5 will have “SVIO +5V” on (orange). The secondary I/O voltage is not configurable.

2.1.3 Primary/Secondary Bus Frequency

The three LEDs labeled CONF66, P66MHz, and S66MHz allow the user to quickly determine the speeds of the primary and secondary bus. Please see section 2.2 for further details.

2.1.4 PCI LEDs

2.1.4.1 Heartbeat (LED4)

The secondary PCI clock SCLK is divided down to form a heartbeat, visible as LED4 on the extender. The sole purpose of the heartbeat is to conveniently indicate that the PCI bridge is functioning. If the secondary bus is running at 66MHz, the blinking frequency is approximately 1 Hz (on for 500ms, off for 500ms). If the secondary bus frequency is 33MHz, the approximate frequency of the LED is 0.5 Hz (on for 1s, off for 1s). If this signal is not cycling on and off, the bridge is not driving SCLK. SCLK is required for the secondary bus to function.

2.1.4.2 PCI Reset (RST-)

The LED marked “RST-” will illuminate when PCI reset (RST-) is active. PCI reset will be active during the initial stages of power-up or if the reset button on the front of the computer is depressed. During normal operation, this LED should be off.

2.1.5 Power Rail LEDs

The following voltages have LEDs:

- VAUX
- +3.3VP (primary +3.3V)
- +3.3V (secondary +3.3V)
2.2 DIP Switch 2: Configuration of Primary/Secondary Bus Frequency of Operation

There are three LEDs labeled CONF66, S66MHz, and P66MHz that are associated with the primary/secondary bus frequency. DIP Switch 2 allows selection of different primary/secondary frequency configurations. Figure 4 shows a diagram of the DIP Switch 2 circuit and Table 2 provides bus frequency settings and associated LED details.

- +5V
- +12V
- -12V

Figure 4. DIP Switch 2 (SW2) Circuitry
### Table 2. Bus Frequency Settings (SW2 on PWB)

<table>
<thead>
<tr>
<th>SW2</th>
<th>Motherboard Frequency</th>
<th>Card Frequency</th>
<th>LED CONF66</th>
<th>LED P66MHz</th>
<th>LED S66MHz</th>
<th>Primary Frequency will be</th>
<th>Secondary Frequency will be</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>on</td>
<td>66</td>
<td>66</td>
<td>on</td>
<td>on</td>
<td>on</td>
<td>66</td>
<td>66</td>
<td>Default: PCI compliant</td>
</tr>
<tr>
<td></td>
<td>66</td>
<td>33</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>66</td>
<td>33</td>
<td>Primary and secondary bus will run at optimal speed</td>
</tr>
<tr>
<td></td>
<td>33</td>
<td>66</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>33</td>
<td>33</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33</td>
<td>33</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>33</td>
<td>33</td>
<td></td>
</tr>
<tr>
<td>off</td>
<td>66</td>
<td>66</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>66</td>
<td>33</td>
<td>Primary bus will run at optimal frequency and secondary bus will run at frequency 1/2 the primary bus frequency</td>
</tr>
<tr>
<td></td>
<td>66</td>
<td>33</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>66</td>
<td>33</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33</td>
<td>66</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>33</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33</td>
<td>33</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>33</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>on</td>
<td>66</td>
<td>66</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>33</td>
<td>33</td>
<td>Primary/secondary bus are forced to run at 33MHz</td>
</tr>
<tr>
<td></td>
<td>66</td>
<td>33</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>33</td>
<td>33</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33</td>
<td>66</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>33</td>
<td>33</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33</td>
<td>33</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>33</td>
<td>33</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Changes made to switch settings on SW2 will be reflected in the firmware when the system is restarted.
3 Power Options and Settings

3.1 Onboard +3.3V Regulator

The DNPCIEXT-S3/5 provides both +5V and +3.3V availability and several options for routing and usage.

An onboard regulator converts the +5V power rail delivered by the host system to +3.3V for use on the extender and by devices installed on the secondary bus. This allows the use of devices that require +3.3V in systems which do have a +3.3V supply. Up to 10A of +3.3V may be drawn, provided the host system delivers enough +5V power. If the host system cannot deliver enough power, an external power supply may be connected to the extender using the P1 connector.

**CAUTION** Regulator heat sinks may be extremely hot.

*Figure 5.* provides a circuit diagram of the voltage selection circuitry and *Table* gives the power specifications for the DNPCIEXT-S3/5 board.

*Figure 5. Voltage Selection Circuit Showing Jumper Pins*

If your host system does not have +3.3V up to 5A of the regulated +3.3V power supply may be driven back onto the +3.3V rail of the host system for use by other devices.

**CAUTION** Do not drive +3.3V onto a system if this power rail is already present; damage to host system, extender, and secondary devices will result.
Verify that the LED marked “+3.3VP” is not lit when the system is on before using this feature. To enable this feature install jumpers across pins 1 and 3 and across pins 2 and 4 on J11. Both jumpers are required to handle the amount of current passed thru them. Current protection is provided by either a 5A single-use fuse or a 2.6A resettable poly switch fuse, depending on configuration (standard configuration TBD).

### Table 3. DNPCIEXT-S3/5 Power Specifications

<table>
<thead>
<tr>
<th>Power</th>
<th>Current Rating (continuous)</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3V</td>
<td>10A</td>
<td>-1%, +2%</td>
</tr>
</tbody>
</table>

3.2 VAUX

Most systems provide an auxiliary power rail, VAUX, regardless of whether the system is powered on. Because this supply is always present, even when the system is turned off, installing or removing PCI devices requires you turn off (usually a switch on the back of computer systems) or unplug the system power supply. The soft switch at the front of most computer cases will not disable the system power supply.

**CAUTION** Failure to remove all power from the system may damage your system, extender, and secondary devices. Also, never add or remove cards or cables from a machine unless all LEDs on the DNPCIEXT-S3/5 are off!

LED’s are provided for all power rails; do not install or remove devices unless all LED’s are off.

VAUX will not be delivered to secondary devices unless J10 is properly installed: to enable VAUX on the secondary bus install jumpers across pins 1 and 3 and across pins 2 and 4 on J10. Both jumpers are required to handle the amount of current passed thru them. Please note that the VAUX LED will not light if the jumpers on J10 are not installed, regardless of the availability of VAUX on the host system.
4 Secondary Slot Numbering and IDSEL Mapping

Per Intel’s design specification, the PCI secondary bus option card slots are mapped to PCI device numbers 4, 5, and 6 as shown in Figure 6. The secondary bus lines $s_{ad<20:22>$ are used as secondary IDSEL lines.

Figure 6. Secondary PCI Slot Numbering
5 Interrupt Routing

Because a total of 12 interrupts are connected to the secondary bus PCI slots (INTA-, INTB-, INTC- and INTD- for each slot), and only four interrupts are driven to the card edge, the 12 incoming interrupts must be combined. This ORing of interrupts is performed in accordance with the PCI-to-PCI Bridge Architecture Specifications. Table 4, lists the ORing of interrupts and Table 5, lists the interrupts from the devices on the secondary slots to the interrupts on the EB154 fingers.

Table 4. Interrupt ORing

<table>
<thead>
<tr>
<th>Device Number</th>
<th>Interrupt Pin on Device</th>
<th>Interrupt PIN on Board Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>INTA-</td>
<td>INTA-</td>
</tr>
<tr>
<td></td>
<td>INTB-</td>
<td>INTB-</td>
</tr>
<tr>
<td></td>
<td>INTC-</td>
<td>INTC-</td>
</tr>
<tr>
<td></td>
<td>INTD-</td>
<td>INTD-</td>
</tr>
<tr>
<td>5</td>
<td>INTA-</td>
<td>INTB-</td>
</tr>
<tr>
<td></td>
<td>INTB-</td>
<td>INTC-</td>
</tr>
<tr>
<td></td>
<td>INTC-</td>
<td>INTD-</td>
</tr>
<tr>
<td></td>
<td>INTD-</td>
<td>INTA-</td>
</tr>
<tr>
<td>6</td>
<td>INTA-</td>
<td>INTC-</td>
</tr>
<tr>
<td></td>
<td>INTB-</td>
<td>INTD-</td>
</tr>
<tr>
<td></td>
<td>INTC-</td>
<td>INTA-</td>
</tr>
<tr>
<td></td>
<td>INTD-</td>
<td>INTB-</td>
</tr>
</tbody>
</table>
### Table 5. Interrupts from Devices to EB 154 Fingers

<table>
<thead>
<tr>
<th>Interrupts from Device on Secondary Slots</th>
<th>Interrupts on EB 154 Fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTA4-</td>
<td>INTA-</td>
</tr>
<tr>
<td>INTD5-</td>
<td></td>
</tr>
<tr>
<td>INTC6-</td>
<td></td>
</tr>
<tr>
<td>INTB7-</td>
<td></td>
</tr>
<tr>
<td>INTB4-</td>
<td>INTB-</td>
</tr>
<tr>
<td>INTA5-</td>
<td></td>
</tr>
<tr>
<td>INTD6-</td>
<td></td>
</tr>
<tr>
<td>INTC7-</td>
<td></td>
</tr>
<tr>
<td>INTC4-</td>
<td>INTC-</td>
</tr>
<tr>
<td>INTB5-</td>
<td></td>
</tr>
<tr>
<td>INTA6-</td>
<td></td>
</tr>
<tr>
<td>INTD7-</td>
<td></td>
</tr>
<tr>
<td>INTD4-</td>
<td>INTD-</td>
</tr>
<tr>
<td>INTC5-</td>
<td></td>
</tr>
<tr>
<td>INTB6-</td>
<td></td>
</tr>
<tr>
<td>INTA7-</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** In the first column of this table, the number after each interrupt pin is the device number of the devices in the secondary slots.
6 Headers

6.1 J8 – IDC Power Header

J8 can be used to probe any of the power rails on the DNPCIEXT-S3/5. Power pins have been purposely left off the other connectors so that probing is less likely to result in damage. Alternatively, an insulation displacement connector (IDC) can be attached to J8 and used to provide power for other uses. Each pin on J8 is capable of supplying approximately 1.0 amp, but this is dependent upon the amount of power available from the motherboard. Figure 7 shows a diagram of connector J8.

Figure 7. J8 IDC Power Header

![Diagram of J8 IDC Power Header]

6.2 Present Header (J6)

The PCI bus defines two pins that allow the host motherboard to determine if a plug-in card is present, and if so, how much power it will draw. The Intel 21154 uses a separate shift register to obtain the “present” status for the secondary slots. This function is rarely used, therefore the shift register necessary to obtain this information was omitted from the extender. The “present” signals for the secondary slots are available on J6, as shown in Figure 8.

Figure 8. J6 Present Header
6.3 CPLD Programming Header (J9)

As shown in Figure 9, J9 is a header that enables programming of the CPLD. Both the power rails +5V and +3.3V are available on the header to provide power to the JTAG cable. The JTAG cable necessary to program the CPLD is not provided with the DNPCIEXT-S3/5. If you wish to reprogram the CPLD, the cable can be obtained from Xilinx. The part number is HW-JTAG-PC. See http://www.xilinx.com/ for more information.

6.4 PCI Signal Header (J5)

Header J5 contains all the PCI signals. Figure 10 shows header J5 and Table 6 lists the PCI signals that are found on J5 in alphabetic order for easy reference.
NOTE  All of the PCI signals listed on J5 of the extender that begin with an ‘S’ are listed in Table 7 without the ‘S’

Figure 10. PCI Signal Header (J5)
### Table 6. J5: Alphabetic Listing of PCI Symbols

<table>
<thead>
<tr>
<th>PCI Signal</th>
<th>Pin # on J5</th>
<th>PCI Signal</th>
<th>Pin # on J5</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACK64-</td>
<td>40</td>
<td>AD52</td>
<td>23</td>
</tr>
<tr>
<td>AD0</td>
<td>41</td>
<td>AD53</td>
<td>24</td>
</tr>
<tr>
<td>AD1</td>
<td>42</td>
<td>AD54</td>
<td>25</td>
</tr>
<tr>
<td>AD10</td>
<td>54</td>
<td>AD55</td>
<td>26</td>
</tr>
<tr>
<td>AD11</td>
<td>53</td>
<td>AD56</td>
<td>27</td>
</tr>
<tr>
<td>AD12</td>
<td>56</td>
<td>AD57</td>
<td>28</td>
</tr>
<tr>
<td>AD13</td>
<td>55</td>
<td>AD58</td>
<td>29</td>
</tr>
<tr>
<td>AD14</td>
<td>58</td>
<td>AD59</td>
<td>30</td>
</tr>
<tr>
<td>AD15</td>
<td>57</td>
<td>AD6</td>
<td>47</td>
</tr>
<tr>
<td>AD16</td>
<td>67</td>
<td>AD60</td>
<td>31</td>
</tr>
<tr>
<td>AD17</td>
<td>70</td>
<td>AD61</td>
<td>32</td>
</tr>
<tr>
<td>AD18</td>
<td>69</td>
<td>AD62</td>
<td>33</td>
</tr>
<tr>
<td>AD19</td>
<td>72</td>
<td>AD63</td>
<td>34</td>
</tr>
<tr>
<td>AD2</td>
<td>43</td>
<td>AD7</td>
<td>48</td>
</tr>
<tr>
<td>AD20</td>
<td>71</td>
<td>AD8</td>
<td>50</td>
</tr>
<tr>
<td>AD21</td>
<td>74</td>
<td>AD9</td>
<td>51</td>
</tr>
<tr>
<td>AD22</td>
<td>73</td>
<td>C/BE0-</td>
<td>49</td>
</tr>
<tr>
<td>AD23</td>
<td>76</td>
<td>C/BE1-</td>
<td>60</td>
</tr>
<tr>
<td>AD24</td>
<td>75</td>
<td>C/BE2-</td>
<td>68</td>
</tr>
<tr>
<td>AD25</td>
<td>80</td>
<td>C/BE3-</td>
<td>78</td>
</tr>
<tr>
<td>AD26</td>
<td>77</td>
<td>C/BE4-</td>
<td>36</td>
</tr>
<tr>
<td>AD27</td>
<td>82</td>
<td>C/BE5-</td>
<td>37</td>
</tr>
<tr>
<td>AD29</td>
<td>84</td>
<td>C/BE6-</td>
<td>38</td>
</tr>
<tr>
<td>AD3</td>
<td>44</td>
<td>C/BE7-</td>
<td>39</td>
</tr>
<tr>
<td>AD30</td>
<td>79</td>
<td>CFG1</td>
<td>52</td>
</tr>
<tr>
<td>AD31</td>
<td>86</td>
<td>CLK08</td>
<td>90</td>
</tr>
<tr>
<td>AD32</td>
<td>3</td>
<td>FRAM-*</td>
<td>65</td>
</tr>
<tr>
<td>AD33</td>
<td>4</td>
<td>GND</td>
<td>1</td>
</tr>
<tr>
<td>AD34</td>
<td>5</td>
<td>GNT0*</td>
<td>81</td>
</tr>
<tr>
<td>AD35</td>
<td>6</td>
<td>GNT1-</td>
<td>89</td>
</tr>
</tbody>
</table>
6.5 Miscellaneous Header (J7)

J7 contains a variety of signals that were not logical candidates for placement on other headers. These are shown in Figure 11, and described in more detail in Table 7.

### Table 6. J5: Alphabetic Listing of PCI Symbols (Continued)

<table>
<thead>
<tr>
<th>PCI Signal</th>
<th>Pin # on J5</th>
<th>PCI Signal</th>
<th>Pin # on J5</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD36</td>
<td>7</td>
<td>GNT2-</td>
<td>91</td>
</tr>
<tr>
<td>AD37</td>
<td>8</td>
<td>GPIO2</td>
<td>96</td>
</tr>
<tr>
<td>AD38</td>
<td>9</td>
<td>GPIO3</td>
<td>98</td>
</tr>
<tr>
<td>AD39</td>
<td>10</td>
<td>INTA-</td>
<td>85</td>
</tr>
<tr>
<td>AD4</td>
<td>45</td>
<td>INTB-</td>
<td>92</td>
</tr>
<tr>
<td>AD40</td>
<td>11</td>
<td>INTC-</td>
<td>87</td>
</tr>
<tr>
<td>AD41</td>
<td>12</td>
<td>INTD-</td>
<td>94</td>
</tr>
<tr>
<td>AD42</td>
<td>13</td>
<td>IRDY-</td>
<td>66</td>
</tr>
<tr>
<td>AD43</td>
<td>14</td>
<td>PAR</td>
<td>59</td>
</tr>
<tr>
<td>AD44</td>
<td>15</td>
<td>PAR64</td>
<td>35</td>
</tr>
<tr>
<td>AD45</td>
<td>16</td>
<td>PERR-</td>
<td>64</td>
</tr>
<tr>
<td>AD46</td>
<td>17</td>
<td>REQO-</td>
<td>88</td>
</tr>
<tr>
<td>AD47</td>
<td>18</td>
<td>REQ1-</td>
<td>93</td>
</tr>
<tr>
<td>AD48</td>
<td>19</td>
<td>REQ2-</td>
<td>95</td>
</tr>
<tr>
<td>AD49</td>
<td>20</td>
<td>RST-</td>
<td>83</td>
</tr>
<tr>
<td>AD5</td>
<td>46</td>
<td>SER-</td>
<td>62</td>
</tr>
<tr>
<td>AD50</td>
<td>21</td>
<td>STOP-</td>
<td>61</td>
</tr>
<tr>
<td>AD51</td>
<td>22</td>
<td>TRDY-</td>
<td>63</td>
</tr>
</tbody>
</table>

NOTE: Signal names on J5 that start with a ‘S’ are listed in this table without the ‘S’
Table 7. Description of Miscellaneous Header Pins

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+3.3V</td>
<td>+3.3V power supply</td>
</tr>
<tr>
<td>2</td>
<td>SPARE1</td>
<td>Connected to the CPLD (no defined function)</td>
</tr>
<tr>
<td>3</td>
<td>+12V</td>
<td>+12V power supply</td>
</tr>
<tr>
<td>4</td>
<td>LED0</td>
<td>PCI bus activity</td>
</tr>
<tr>
<td>5</td>
<td>-12V</td>
<td>-12V power supply</td>
</tr>
<tr>
<td>6</td>
<td>LED1</td>
<td>PCI bus activity</td>
</tr>
<tr>
<td>7</td>
<td>+5V</td>
<td>+5V power supply</td>
</tr>
<tr>
<td>8</td>
<td>LED2</td>
<td>PCI bus activity</td>
</tr>
<tr>
<td>9</td>
<td>DP3</td>
<td>SW1, dip switch 3 (no defined function)</td>
</tr>
<tr>
<td>10</td>
<td>LED3</td>
<td>PCI bus activity</td>
</tr>
<tr>
<td>11</td>
<td>+3.3VP</td>
<td>+3.3V volt power supply from primary PCI connector</td>
</tr>
<tr>
<td>12</td>
<td>LED4</td>
<td>Heart Beat (derived from SCLK)</td>
</tr>
<tr>
<td>13</td>
<td>VAUX</td>
<td>VAUX power supply</td>
</tr>
<tr>
<td>14</td>
<td>BSRST*</td>
<td>Buffered SRST* (secondary reset)</td>
</tr>
<tr>
<td>15</td>
<td>BPVIO3.3</td>
<td>Primary I/O voltage is +3.3V (TTL signal from CPLD)</td>
</tr>
<tr>
<td>16</td>
<td>+SVIO</td>
<td>Secondary voltage I/O (will be +3.3V or +5V)</td>
</tr>
<tr>
<td>17</td>
<td>BPVIO5</td>
<td>Primary I/O voltage is +5V (TTL signal from CPLD)</td>
</tr>
<tr>
<td>18</td>
<td>SPARE0</td>
<td>Connected to the CPLD (no defined function)</td>
</tr>
<tr>
<td>19</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>
7 Errata

7.1 Lock-

The functionality associated with the PCI signal LOCK* was deleted in version 2.2 of the PCI specification. Some systems do not connect LOCK* and the unconnected pin does not have a pull-up. If LOCK* floats, noise can cause this signal to go to an asserted state, which corrupts the Intel 21154 bridge. Since this can cause unpredictable PCI behavior, this extender has a pull-up installed on this signal. This is a violation of the PCI specification but will not adversely affect operation. If a secondary device does not work when installed in the host system but does when installed in the extender, the absence of LOCK* in the host system is a possible cause.

7.2 Startup Problems with 21154

The Intel 21154 PCI bridge has known initialization issues at power-up. If no clock appears on SCLK, some registers internal to the 21154 do not get reset, and the result is that no SCLK’s appear. One of the SCLK’s is fed back to the 21154 as the source for the secondary PCI clocks. If no SCLK’s appear, no secondary clocks appear, and the secondary bus does not function. To work around the problem, the necessary clocks are provided to the input SCLK at power-up via a separate oscillator and a quick switch. Contact The Dini Group if you ever see the DNPCIEXT-S3/5 come up in a state where the SCLK’s are not toggling.
8 Assembly Drawing

Figure 12. shows the details for the board’s assembly.

Figure 12. DNPCIEXT Assembly Drawing
9 Ordering Information

Should any additional DNPCIEXT boards or kits be needed, refer to Table 8, for the board description, part number, and price.

Table 8. Available DNPCIEXT Boards and Kit

<table>
<thead>
<tr>
<th>Description</th>
<th>Part Number</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>66MHz, 64-bit Active PCI Extender Card +5V I/O on secondary PCI bus</td>
<td>DNPCIEXT-S5</td>
<td>$549.00</td>
</tr>
<tr>
<td>66MHz, 64-bit Active PCI Extender Card +3.3V I/O on secondary PCI bus</td>
<td>DNPCIEXT-S3</td>
<td>$549.00</td>
</tr>
<tr>
<td>Both DNPCIEXT-S3 and DNPCIEXT-S5 ordered simultaneously</td>
<td>DNPCIEXT-DUAL KIT</td>
<td>$995.00</td>
</tr>
</tbody>
</table>
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